

KNOWLEDGE PROBE 6: PROGRAMMABLE LOGIC DEVICES

Testing and Troubleshooting PLDs

Learning Objectives

1. Identify steps involved in testing PLDs.
 2. Identify components used in testing PLDs.
 3. Describe what to do if a PLD is not operating correctly.
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1. Complex PLDs are often tested automatically by special test equipment.
 - a. True
 - b. False
 2. Where does a JTAG interface usually reside?
 - a. Inside a JTAG chip
 - b. Inside a logic analyzer
 - c. Inside the pattern generator
 - d. Inside the PLD
 3. What is the name given to the test procedure performed by a JTAG interface?
 - a. ATE
 - b. Boundary scan
 - c. Programmable I/O
 - d. Test in/ test out
 4. What pin on a JTAG interface accepts the test inputs?
 - a. TCK
 - b. TDI
 - c. TDO
 - d. TMS
 5. How is the test results read?
 - a. Count clock pulses
 - b. Observe data on the TDO line
 - c. On a logic analyzer
 - d. On an oscilloscope
 6. What is the type of logic circuit used in the JTAG interface to input and output data?
 - a. 3-state I/O
 - b. Counter
 - c. Multiplexer
 - d. Shift register



7. How does the JTAG interface know what to do?
 - a. All functions are preprogrammed
 - b. It is determined by to which internal circuits the JTAG interface is connected
 - c. It receives an instruction code
 - d. The test engineer designs special procedures
8. Boundary scan is desirable because
 - a. Access is provided to points in the IC not brought out at pins
 - b. Testing is faster
 - c. Testing is simplified
 - d. All of the above
9. If an OTP PLD is found bad, the primary course of action is
 - a. Replace it
 - b. Reprogram it