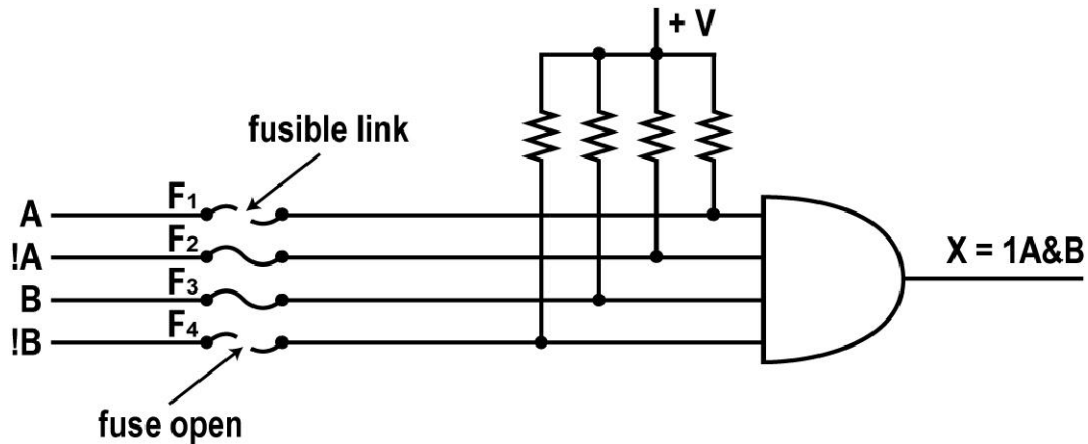


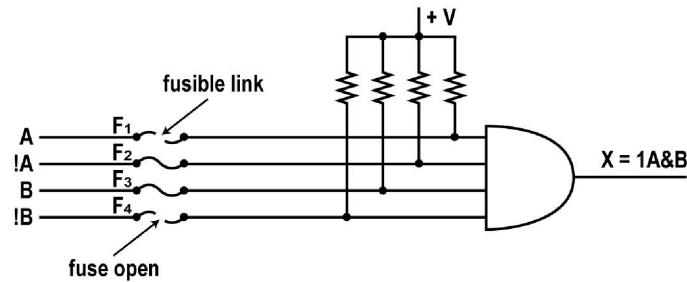
How Programming Is Accomplished

Fusible Links



The earliest form of programmable technology used fuses to connect or not connect the input to a gate. Note that there are two inputs, A and B. The NOT versions !A and !B are also available. All of these signals are simultaneously connected to the inputs to the AND gate by the fuses which are manufactured on the silicon chip with the circuits.

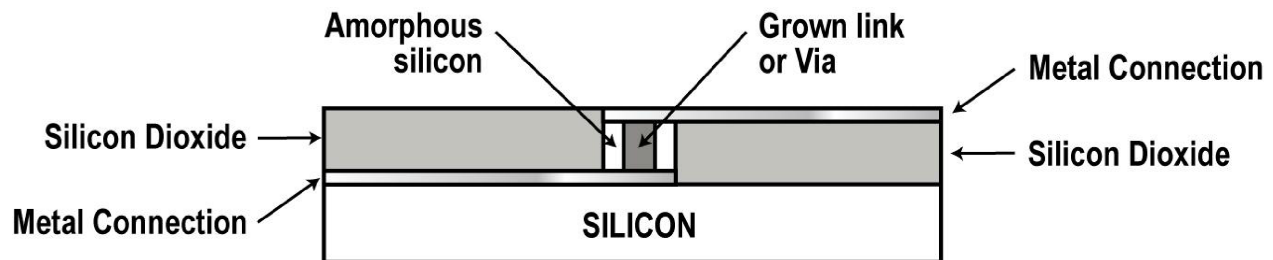
Fusible Links Operation



To program the connections, the undesired inputs are disconnected from the gate by “blowing” the appropriate fuse. This is accomplished by passing a high current through the fuse until it opens. The pull up resistors at the input to the gates make sure that there is a binary 1 on the unused inputs. The fuses of the desired inputs are left connected.

For example, the Boolean equation $X = !A \& B$ is implemented by blowing fuses F1 and F4. In commercial PLDs, this concept is extended to many more inputs on more gates and on the inputs to OR gates in some devices.

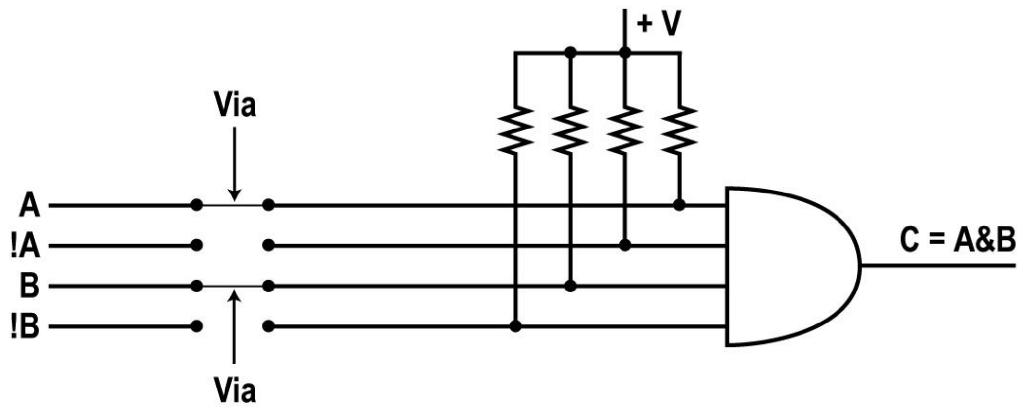
Antifuse Links



An antifuse is the opposite of a fuse. A fuse is initially a short or a low resistance connection that can be opened during programming. An antifuse is initially an open circuit or very high resistance meaning no connection is made. Programming an antifuse causes the open circuit to become a short or an actual connection.

The antifuse is made with standard silicon processing techniques. A small piece of amorphous silicon between two metal layers in the IC serves as an insulator.

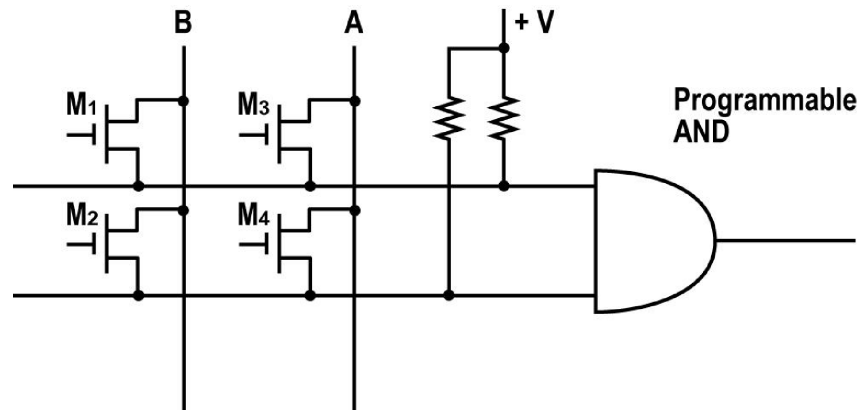
Antifuse Links Operation



When programmed by applying a voltage between the two metal connections, the amorphous silicon is transformed into a low resistance polysilicon link as shown in the figure in the previous slide. The process is known as “growing” a link or connection. The resulting connection is sometimes referred to as a via. Once the via has been grown it is permanent thus these are OTP devices like the fusible links.

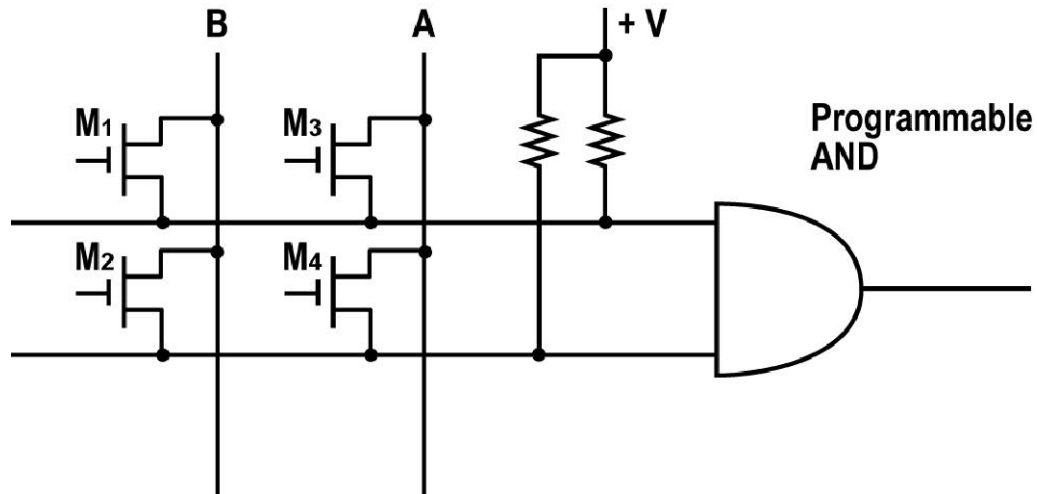
The figure shows how the expression $C = A \& B$ is made.

MOSFET Links



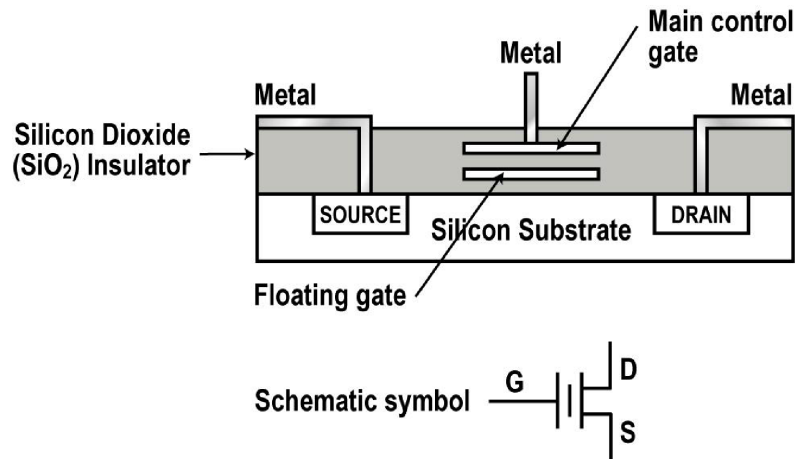
Since all PLDs are CMOS, a MOSFET is often used to create a link between an input or output and another circuit. The figure shows a MOSFET that can be turned off or on to connect to or disconnect from the A or B inputs to the AND gate. There is a MOSFET at the intersection of each AND input and each logic input. The appropriate MOSFET is turned off or on to create the desired programming.

MOSFET Links Operation



If MOSFET M₃ is turned on by applying a positive voltage or binary 1 to the gate, the A input is connected to upper AND input. If MOSFET M₃ has a binary 0 or ground applied to its gate, the MOSFET is off so the data line is pulled up to binary 1 by the pull up resistor thereby enabling the AND gate for other inputs. The issue is, how are the MOSFETs programmed to be on or off?

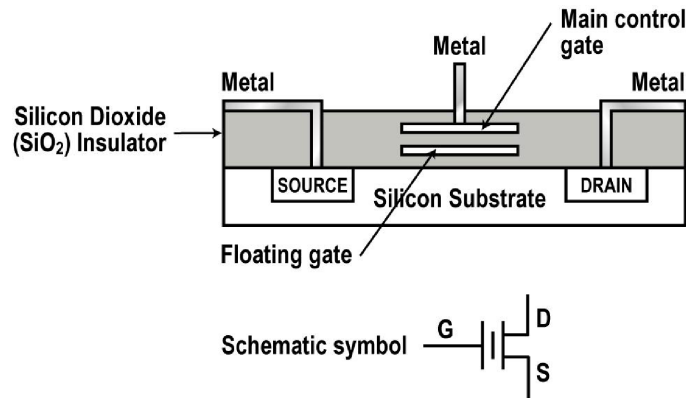
Programmable MOSFET



The arrangement shown in the previous slide can be made with a floating gate MOSFET like those used in erasable programmable read-only memories (EPROM).

This figure shows the cross section of a standard enhancement mode MOSFET but there is a floating gate between the regular control gate and the substrate.

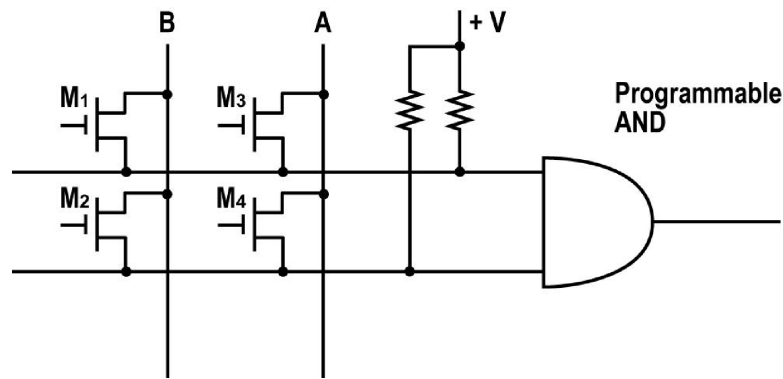
Charging the Floating Gate



To program this transistor, a high voltage is applied between the drain and main gate. This causes electrons to tunnel through the oxide insulator and place a negative charge of electrons on the floating gate. This blocks the effect of the main gate so that the transistor cannot be turned on.

Once the floating gate is charged, it remains charged even if power is turned off. The charge can remain for years making this device an ideal one for making read-only memories (ROMs). Charging the gate programs the MOSFET to be off.

Programmable MOSFET Operation



Now imagine that all the MOSFETs as shown are of the floating gate variety. All MOSFETs are initially unprogrammed and a positive voltage is applied to each gate turning on all MOSFETs and connecting all logic inputs to all AND inputs.

To program the circuit, selected MOSFETs are programmed by charging their floating gates thereby turning them off leaving the desired logic inputs connected to the AND inputs.

The floating gate MOSFETs form a programmable ROM.

Erased Programmable MOSFETs

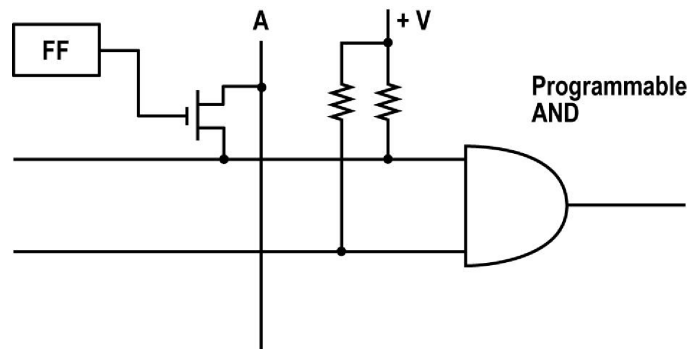
The floating gate MOSFET can be de-programmed by applying ultra violet light to it. That is how the early PROMs worked but such devices are no longer used.

An electrically erasable version was developed and it can be erased by applying a logic signal to an external control line which discharges the floating gate.

Such devices are referred to as electrically erasable programmable read-only memories (EEPROM or E²PROM).

A faster version of the EEPROM is the flash memory which can be erased and reprogrammed faster. It also provides for just erasing and reprogramming portions of the memory rather than all of it.

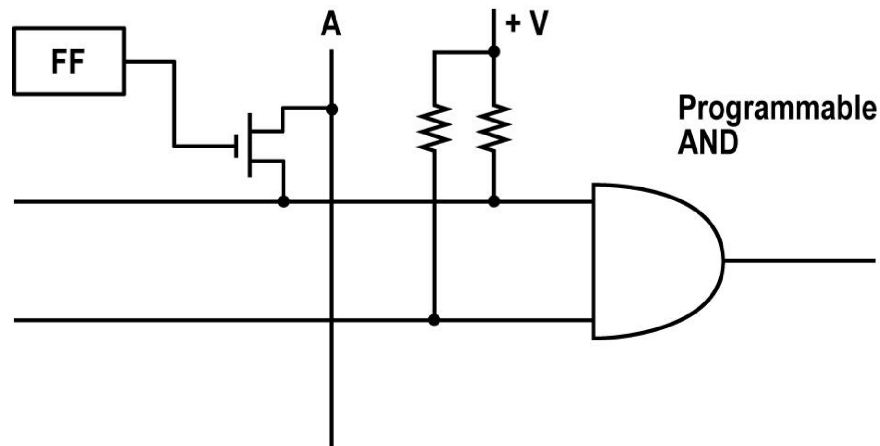
RAM Programmable



The control MOSFETs shown earlier can also be turned off or on by connecting them to flip flops (FFs). If the FF is set, the MOSFET is on and the A input is connected to the upper AND input. If the FF is reset, the MOSFET is off and the AND input is held high by the pull up resistor.

The FF is usually one storage cell of a static random access memory (SRAM). A random access memory is a collection of FFs that are usually arranged as a group of locations to store binary words of a specific length (8-bits, 16-bits, etc.). A decoder is provided to access each word or FF. That FF is then either set or reset to turn the MOSFET off or on as required by the logic.

SRAM Controlled MOSFETs



Most of the newer CPLDs and FPGAs are programmed with SRAM controlled MOSFETs.

The main issue with this arrangement is that when power is turned off, the programming bits in the FFs are lost. On power up, a CPLD or FPGA using this technique must be loaded with the correct code to determine the logic configuration of the chip.

Programming Summary

Fusible links are the main programming method of SPLDs like PROMs, PALs, and PLAs. Antifuses are also used. Both are OTP devices.

Floating gate EPROMs and EEPROMs are used in some SPLDs and CPLDs. Some versions of FPGAs also use this programming method.

SRAM programmable MOSFETs are the primary method of programming FPGAs and some CPLDs.

Programming methods vary widely with the manufacturer as well as the type of chip.

Test your knowledge

Programmable Logic Devices Knowledge Probe 3 How Programming Is Accomplished

Click on [Course Materials](#) at the top of the page.
Then choose **Knowledge Probe 3**.