



Programmable Logic Devices

1. What do programmable logic devices (PLD) do?
 - a. Implement analog circuits
 - b. Implement digital circuits
 - c. Implement both digital and analog circuits
 - d. None of the above
2. The earliest digital logic circuits were made with
 - a. IC's
 - b. MOSFETs
 - c. Sand
 - d. Vacuum tubes
3. Why did IC logic circuits become popular so quickly?
 - a. Because a single chip could hold a complete functional circuits
 - b. Because each chip contained 2 gates or flip flops
 - c. Because the circuits became simpler with time
 - d. Because vacuum tubes were no longer available
4. In the early days, the most popular logic circuits were the
 - a. 7400 bipolar TTL
 - b. CMOS 7400
 - c. ECL 2000
 - d. RCA 4000
5. The medium scale TTL IC's contained
 - a. Counters
 - b. Decoders
 - c. Multiplexers
 - d. All of the above
6. The CMOS version of the 7400 contained
 - a. All the small scale functions of TTL
 - b. All the medium scale functions of TTL
 - c. All the small and medium scale functions of TTL
 - d. None of the functions of TTL
7. In low speed applications, logic operation can be done by
 - a. A single CMOS device
 - b. Designing an ASIC
 - c. Programming a microprocessor
 - d. Programming a PLD



8. Microcontrollers are _____ on a single chip.
 - a. Complete computers
 - b. CPU's
 - c. Input and output circuits
 - d. Memory devices
9. Programmable logic devices can reduce the
 - a. Amount of memory needed
 - b. Amount of power used
 - c. Number of engineers needed
 - d. Number of ICs used
10. For high volume applications, complex circuits can be designed using
 - a. ASICs
 - b. PALs
 - c. Programmable microprocessors
 - d. Several CMOS devices
11. What are the two general categories of logic circuits?
12. In _____ ASICs, the designer takes his circuit to a semiconductor manufacture to produce the IC from scratch.
 - a. Full custom
 - b. Gate array
 - c. Standard cell
 - d. Structured
13. ASIC's are usually very cheap to design and manufacture.
 - a. True
 - b. False
14. A _____ is a small scale PLD made up of AND and OR gates.
 - a. Complex PLD
 - b. FPGA
 - c. Simple PLD
 - d. Standard cell
15. A complex PLD contains multiple _____ which can be interconnected to create a more complex function.
 - a. Field programmable PLDs
 - b. Gate arrays
 - c. Simple PLDs
 - d. Standard cells



16. FPDs are larger devices, which contain _____ cells, which store information that turn circuits on or off.
 - a. Decoder
 - b. Large
 - c. Memory
 - d. Microprocessor
17. Which field programmable device is able to compete with the performance of the ASICs?
 - a. CPLD
 - b. FPGA
 - c. PLA
 - d. SPLD
18. When produced in volume, embedded controllers are about
 - a. A few dollars each
 - b. A few hundred dollars each
 - c. A few cents each
 - d. Extremely expensive
19. Large printed circuit boards are now being reduced to
 - a. 5 single ICs
 - b. A system on a single chip
 - c. Smaller populated circuit boards
 - d. The size of an atom
20. A PLD can produce the desired Boolean function by
 - a. Connecting all the AND gates in series
 - b. Creating a program in C language
 - c. Hardwiring all individual circuits
 - d. Turning individual circuits on or off
21. PLDs are made of AND and OR gates connected in
 - a. Parallel
 - b. Product-of-sums format
 - c. Series
 - d. Sum-of-products format
22. In the SOP format, all inputs are connected to
 - a. AND gates
 - b. Inverter gates
 - c. NOR gates
 - d. OR gates



23. More advanced PLDs contain
- Inverters
 - Microprocessors
 - NAND gates
 - RAM
24. In programmable read-only memory (PROM), the data
- Can be reprogrammed once
 - Can be reprogrammed several times
 - Is permanently stored in it
 - Will be lost if power is removed
25. In the PROM, the inputs are decoded by a fixed _____ array.
- AND
 - AND and OR
 - NAND
 - OR
26. Logic circuits can be designed from _____ instead of Boolean equations.
- Fact tables
 - Honest forms
 - Logic tables
 - Truth tables
27. In a _____, the AND and OR arrays are both programmable.
- NAND array
 - PAL
 - PLA
 - PROM
28. In a/an _____, the inputs to the AND gates are programmable but the inputs to the OR gates are fixed.
- ASIC
 - PAL
 - PLA
 - PROM
29. Flip flops are sometimes connected to the PLDs output in order to
- Reduce the Boolean equation
 - Select the source of the output
 - Speed up the propagation delay
 - Store the output data



30. Performance is determined by the _____ the propagation delays for each logic circuit.
- Difference in
 - Product of
 - Smallest of
 - Sum of
31. The earliest form of programming was done with
- Antifuses
 - Fuses
 - Open circuits
 - None of the above
32. Undesired inputs are disconnected by
- Applying high current to blow the fuse
 - Applying high voltage to form a fuse
 - Cutting the jumper cables
 - Removing the solder connection
33. The purpose of the pull up resistor is to
- Ensure the input is grounded
 - Ensure there is a binary 1 on the unused input
 - Pull up the current level
 - Reduce the overall resistance of the circuit
34. Antifuse links initially start out as a/an
- Binary zero
 - Low resistance
 - Open
 - Short
35. When an antifuse is programmed, the amorphous silicon turns into a
- Fusible link
 - High resistance polysilicon
 - Low resistance polysilicon
 - Silicon dioxide
36. What is another name for the programmed antifuse link?
- Duct
 - Levee
 - Tunnel
 - Via



37. In PLDs, _____ are often used to create the link between input/output and another circuit.
- AND gates
 - BJTs
 - Inverters
 - MOSFETs
38. Charging the floating gate will program the MOSFET to be
- On
 - Off
39. When power is removed from a floating gate, the floating gate
- Can remain charged for years
 - Immediately loses its charge
 - Will lose its charge within 24 hours
 - Will lose its charge within 8 hours
40. In earlier days, how were floating gate MOSFETs de-programmed?
- With high voltage
 - With fusible links
 - With ultra violet light
 - With low intensity light
41. Most CPLDs and FPGAs are programmed with _____ controlled MOSFETs.
- Current
 - Fuse
 - SRAM
 - Voltage
42. A CPLD has multiple PALs and is used for
- Large, more sophisticated applications
 - Medium sized applications
 - Military applications only
 - Simple applications
43. In a generic block diagram of a CPLD, the PALs are part of the
- I/O circuit
 - Interconnect matrix
 - Logic blocks
 - Multiplexer
44. Logic blocks can have a wide variation in their configurations.
- True
 - False



45. The intellectual property of a FPGA design can be protected by using
- An EEPROM to initialize the FPGA
 - Storing the program configuration into SRAM storage cells
 - Using an external ROM to initialize the FPGA
 - Using SRAM to initialize the FPGA
46. A LUT can be programmed by setting or resetting a _____ to create the desired output.
- Decoder
 - Flip flop
 - Inverter
 - MUX
47. Most FPGAs use a _____ input LUT.
- 2
 - 3
 - 4
 - 10
48. What is the word length for a 32 x 4 SRAM block?
- 4 bits
 - 8 bits
 - 16 bits
 - 32 bits
49. Newer FPGAs include a MAC circuit which
- Increases the memory
 - Is an embedded controller
 - Performs arithmetic operations
 - Stores more data
50. The Flex 10K architecture includes embedded array blocks (EABs) which are
- Blocks of SRAM cells with registers on the input and output
 - Embedded microcontrollers with two or more inputs
 - For interconnect paths for very large applications
 - Rarely used in modern applications
51. A PLD development system is used to
- Build the PLD hardware
 - Design the development board
 - Program the PLD
 - All of the above



52. The PLD to be programmed is plugged into a
- Development board
 - Personal computer
 - Serial interface
 - Wall outlet
53. Early PLD development software used
- Dynamic entry
 - Flow chart software
 - Multisim
 - Schematic entry
54. What is a netlist?
- List of errors found by the PLD
 - List of special characters used by the PLD
 - Programming language used to program the PLD
 - Text file which defines the interconnectivity of a circuit
55. Modern PLDs are designed and programmed with
- Assembler language
 - Hardware description language
 - Multiple language code
 - Schematic entry
56. Which hardware description language is now a formal IEEE standard?
- CUPL
 - PALASM
 - Schematic entry
 - Verilog
57. What does the first part of an HLD code always define?
- Beginning and end statements
 - Logic operations
 - Names of the inputs and outputs
 - SOP format
58. Most HDL code must be entered in
- Combination of SOP and POS forms
 - Product of sums form
 - Sum of products form
 - Any of the above



59. Once the design has been entered in the PLD, the software will compile it and produce a/an _____ code.
- Duplicate
 - Logic
 - Object
 - Reduction
60. Functional verification is done by the
- Compiler
 - Logic code
 - PLD itself
 - Simulator on the PC
61. A JTAG defined test procedure is called a/an
- Boundary scan
 - Logic analyzer
 - Output protocol
 - Vertical scan
62. A boundary scan cell can allow inputs from either the _____ or an applied test input.
- Multiplexer
 - Normal data inputs
 - Switches
 - Test access port
63. Test bit patterns can be loaded into the BSC from an external source called
- External pattern generator
 - Shift register
 - Test access port
 - Test data input
64. The test access port (TAP) controller
- Allows only select inputs into the BSC
 - Controls the boundary scan process
 - Controls the development software
 - Is used to collect test data