

## KNOWLEDGE PROBE 5: PROGRAMMABLE LOGIC DEVICES

### Programming PLDs

#### Learning Objectives

1. Describe the design process used in programming PLDs.
  2. Identify programming languages and coding used in programming PLD.
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1. Which of the following is NOT usually a part of a PLD development system?
    - a. PC
    - b. PLD chip
    - c. Printer
    - d. Programmer
  2. What software is most commonly used to create the desired logic for a PLD?
    - a. C+ language
    - b. HDL
    - c. MultiSim
    - d. Schematic capture
  3. Most FPGAs use a programming language called
    - a. ABEL
    - b. CUPL
    - c. PALASM
    - d. VHDL
  4. Verilog is a
    - a. Company name
    - b. FPGA HDL
    - c. PAL programming language
    - d. Type of PLD
  5. Which is true if a logic design is in POS instead of SOP?
    - a. Circuit must be redesigned
    - b. deMorgan's theorem is used to convert POS to SOP
    - c. Karnaugh maps are used to convert POS to SOP
    - d. Logic cannot be implemented
  6. What is used to test the logic before it is down loaded to the PLD?
    - a. Compiler
    - b. Net list
    - c. Simulator
    - d. Synthesizer



7. The two types of verification performed by a HDL are
  - a. Functional and timing
  - b. POS and SOP
  - c. Schematic vs. truth table
  - d. Speed and power consumption
  
8. What part of the HDL converts the design to the PLD bit patterns?
  - a. Compiler
  - b. Net list
  - c. Simulator
  - d. Synthesizer