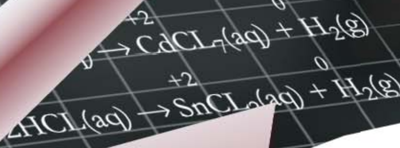
TEACHERS GUIDE

SEMICONDUCTOR SCIENCE ACTIVITIES FOR HIGH SCHOOL CHEMISTRY

CHEMISTRY



MARICOPA COMMUNITY COLLEGES

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National Science Foundation

MARICOPA COMMUNITY COLLEGES

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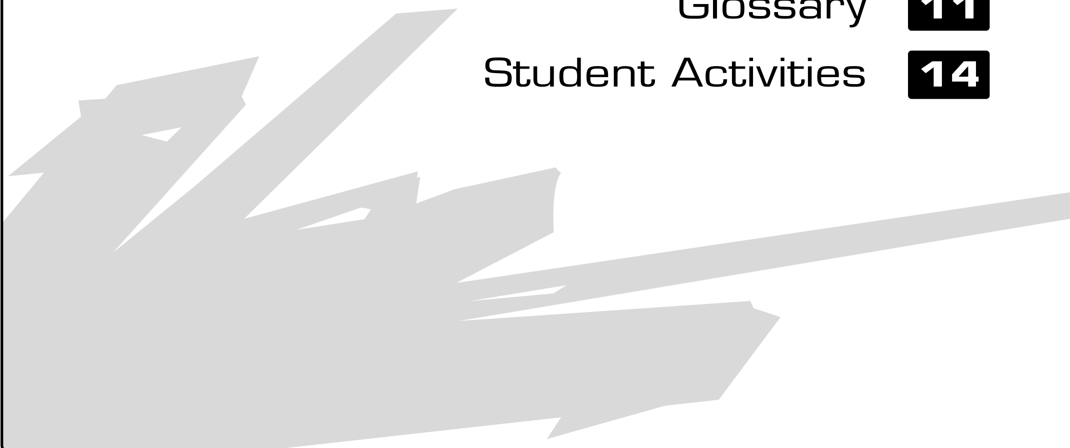
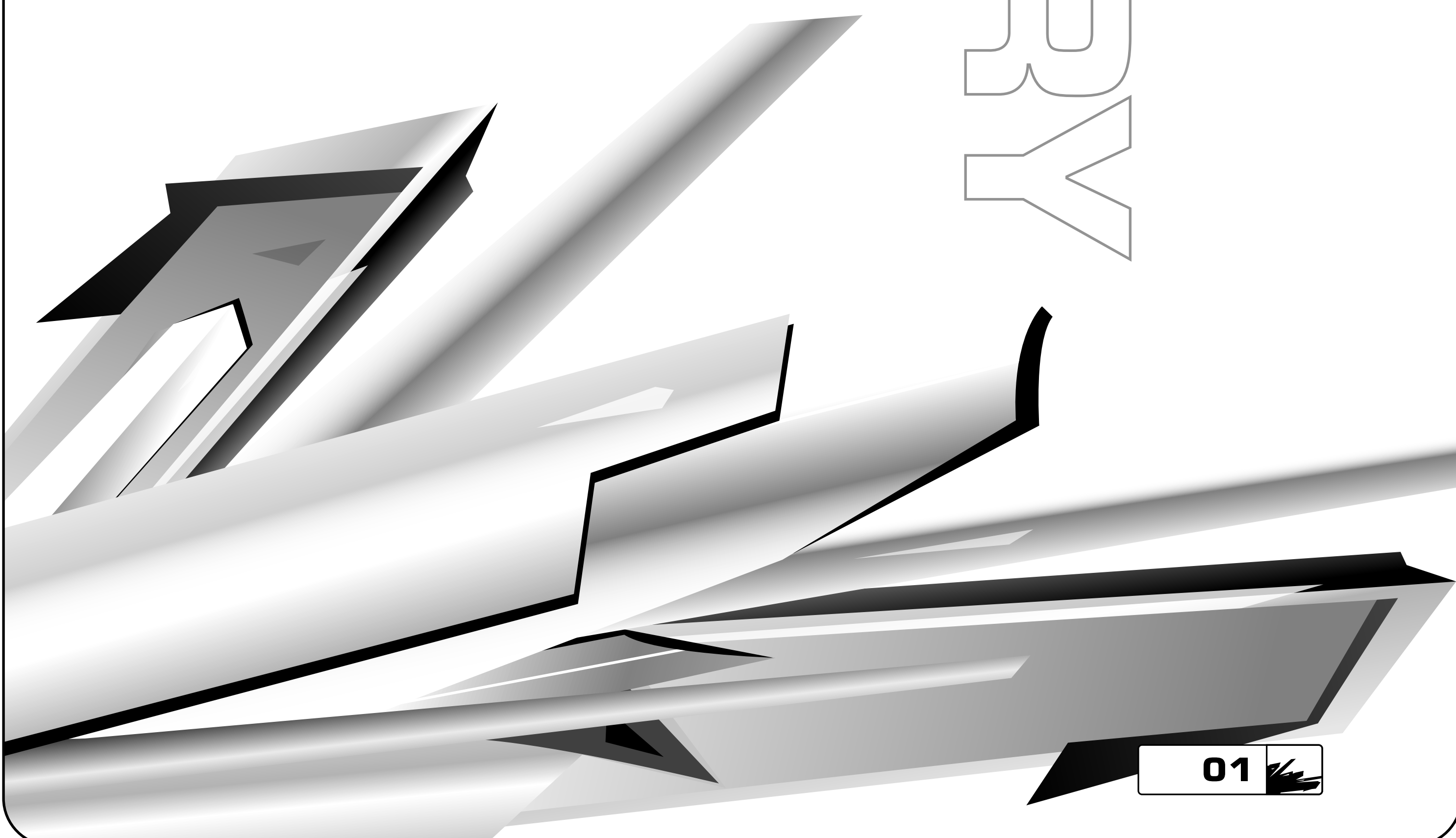


CHEMISTRY

Semiconductor Science Activities for High School Chemistry

The student activities in this packet are designed to be incorporated into a standard high school chemistry curriculum. The intent is to provide the student with an introduction to study of the facets of chemistry as they apply to semiconductor technology.



Introducing Semiconductor Science

Semiconductor Science is a curriculum resource that helps physics and chemistry teachers introduce semiconductor manufacturing processes to their high school students. The purpose of the resources is fourfold:

1. Support high school level physics, chemistry and math education
2. Promote hands-on learning experiences in science,
3. Demonstrate applications of science in the "real" world,
4. Foster interest in the semiconductor industry as a career option.

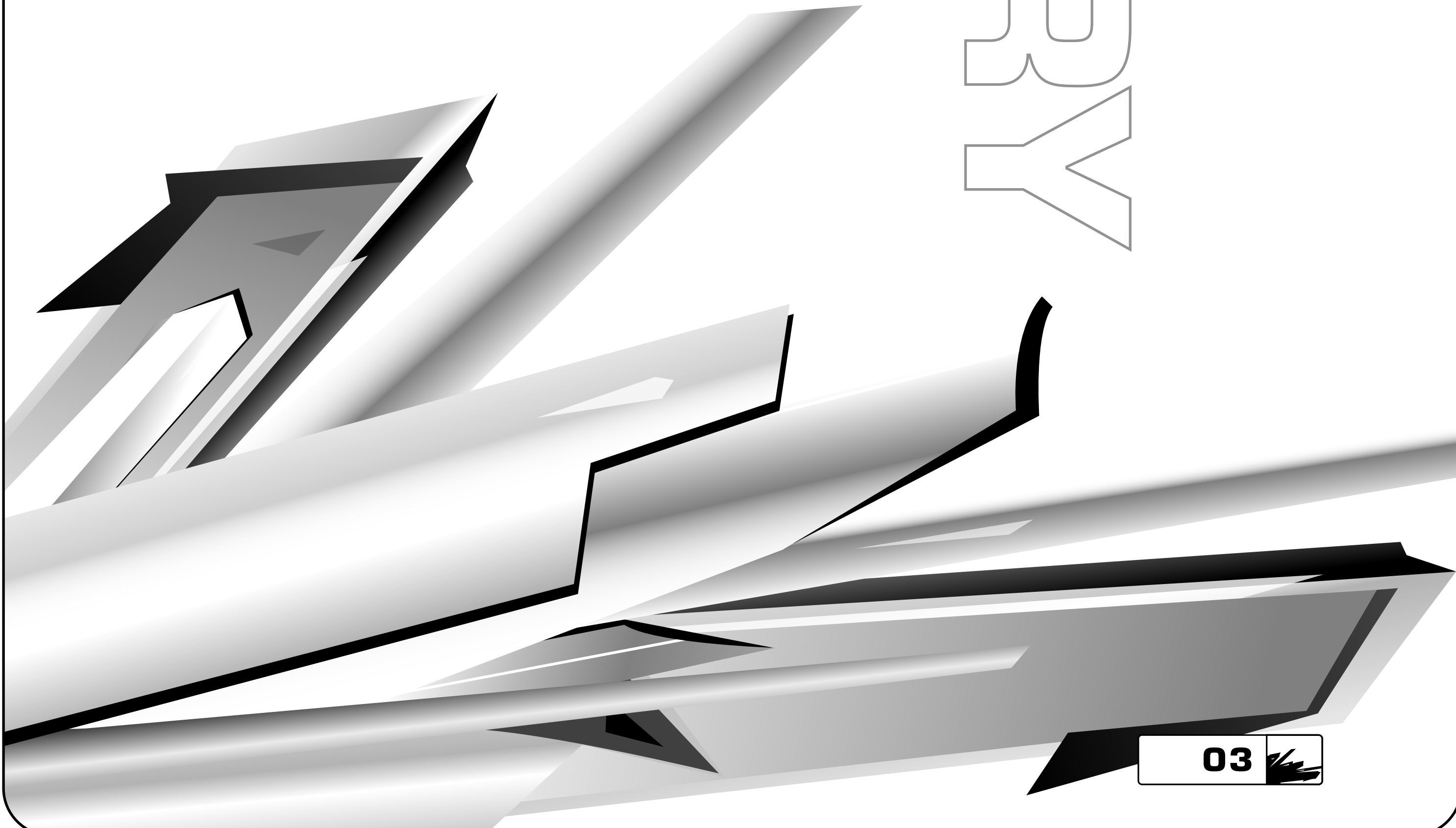
Because semiconductor manufacturing is filled with relevant examples that educators can use to illustrate the "real-world" utility of scientific concepts, Semiconductor Science can be used to enhance an already existing curriculum or stand alone as a science-based introduction to semiconductor manufacturing. Teaching resources available through MATEC include:

1. The video, "A Fab Way to Work"
2. Background information on semiconductor manufacturing
3. Curriculum modules containing:
   a. Lesson objectives that relate to the traditional curriculum
   b. A list of materials that are used in the lesson
   c. Lecture/discussion notes
   d. Student activities that simulate semiconductor manufacturing processes
   e. Directions for conducting assessment
   f. Suggestions for enrichment
   g. A list of related resources for teachers and students
4. Overheads and other instructional support pieces
5. Student activity sheets and supplies
6. Assessment tools
7. Career awareness materials for students, parents and educators
8. A hands-on physics and chemistry kit

Semiconductor Science was developed through Maricopa Advanced Technology Education Center (MATEC), a clearinghouse for instructional aids in the semiconductor industry. This booklet contains preliminary drafts of some of the print materials to be included in the kit and is for presentation purposes only.

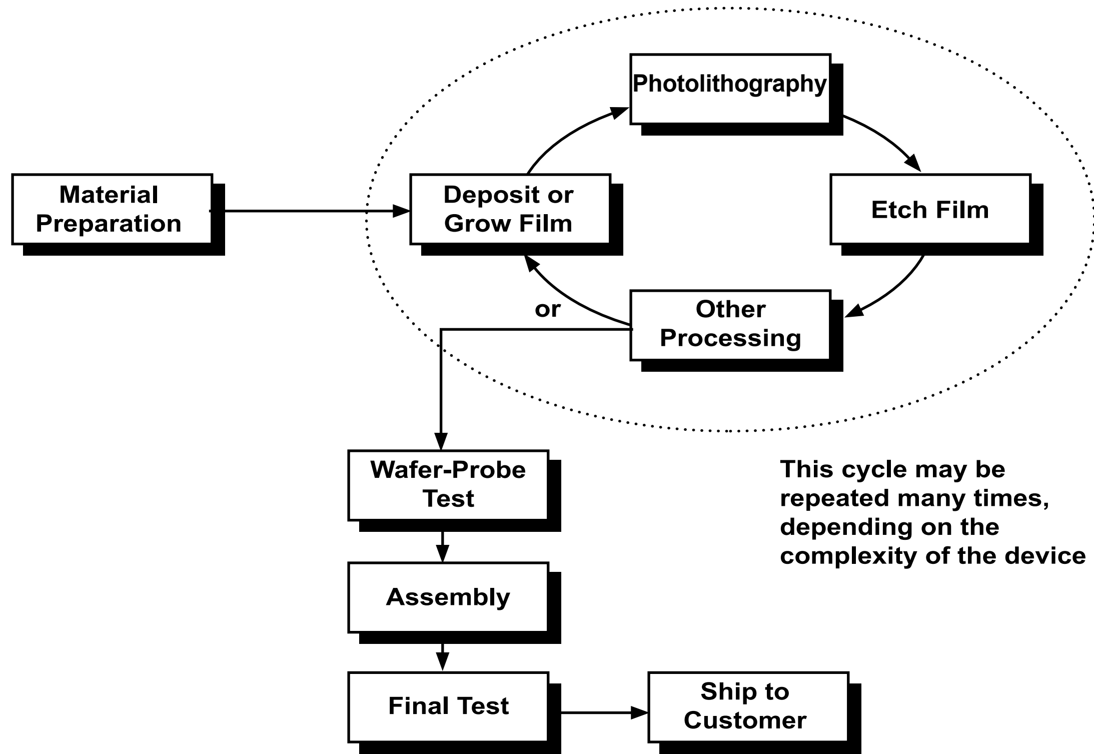
Background Information on Semiconductor Manufacturing

CHEMISTRY



Background Information on Semiconductor Manufacturing

The following diagram is a schematic of the sequence of steps involved in semiconductor processing.



Material Prep:

Polysilicon Manufacture → Crystal Growth: Single Crystal → Wafer Preparation: High Quality Wafers

Three main steps:

A. Purification of silicon:

The initial step in the production of wafer grade silicon is to mix silicon dioxide (sand) with wood and coke at 1600ºC to give 98% (2 parts per 100) pure metallurgical grade silicon (MGS). Since silicon purity is essential, a second step is added to produce electronic grade silicon (EGS). MGS is added to gaseous dry HCl to form trichlorosilane ($HSiCl_3$) and hydrogen gas. This mixture is separated by fractional distillation, similar to the separation methods used in gasoline production. The trichlorosilane is then reacted with hydrogen gas to produce HCl and EGS, which is separated using chemical vapor deposition methods. EGS is 99.9999% pure (2 parts per billion).

B. Growing the silicon ingot

Raw EGS is polysilicon and does not have the correct crystal structure. Raw EGC with any dopants desired for the electrical specifications for the wafer are

placed into a crucible and heated to the melting point of silicon (1200ºC). The Czochralski method is used in crystal production. A large crucible is loaded with polycrystalline chunks of the semiconductor material and small amounts of dopant. The polycrystalline silicon chunks and dopants are heated to a liquid state. Then a seed crystal is introduced that has the same orientation as the desired final larger crystal (i.e. <100>, >111?). To achieve crystal perfection, uniform doping, and diameter control, the crucible and seed are rotated in opposite directions. The crystal growth is then slowly lifted out of the melted material to form an ingot 8 to 10 feet long of a diameter up to 12 inches depending on wafer specifications.

C. Preparation of the ingot:

The ends of the ingot are removed, lathed to precise roundness and the diameter checked for exactness to specifications. The crystal orientation is checked using x-ray crystallography. X-rays are diffracted and scattered by the regular arrangement of atoms, molecules, or ions in a crystal. The diffraction pattern is recorded as dark spots where the diffracted x-rays strike a photographic plate. Measurements can be made of the pattern of dark spots on the film and working backwards the arrangement of the particles that produced the diffraction can be found.

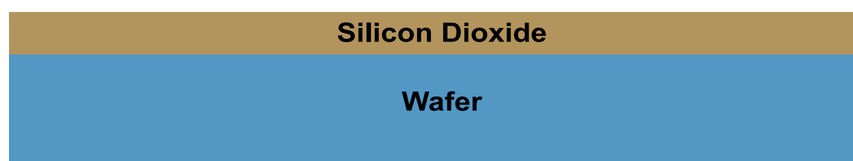
The material properties of the crystal will change with different crystal orientations. The axis of orientation determines the type devices that can be fabricated from the silicon crystal.

A flat surface is ground along the length of the wafer. A few wafers are cut from the ingot for measurement and testing. These slices are tested for thickness, diameter, flatness, and uniform electrical resistance. Once these wafers are found to meet specifications the ingot is sliced to create individual wafers, 20-30 mils thick, using a diamond-edged, inner diameter saw.
The individual wafers are washed in de-ionized water, edges are ground to reduce chips in later steps, and the wafer surfaces are ground to 2 micron uniform flatness and polished to a mirror-like finish. The wafers are cleaned using hydrogen peroxide and ammonium hydroxide followed by de-ionized water rinse to remove inorganic and organic material. Metal contaminants are removed using hydrogen peroxide and hydrochloric acid with a de-ionized water rinse. The wafers are now considered to be high quality, prepared to meet customer specifications, and are shipped to the customer.

Deposit or Grow film:

A. Oxidation: An oxide is grown on silicon for one of the following reasons:

1. a mask for protection during diffusion or ion implantation.
2. a gate oxide in MOS devices.
3. a field oxide for device isolation.
4. a protective layer for the finished device.
5. interlayer dielectric (an insulating material between the plates of a capacitor).



Oxidation Layering

B. Thin film deposition: Thin films may be metals, semiconductors, or insulators. Films may be used as temporary protective layers or to construct circuit or device components.

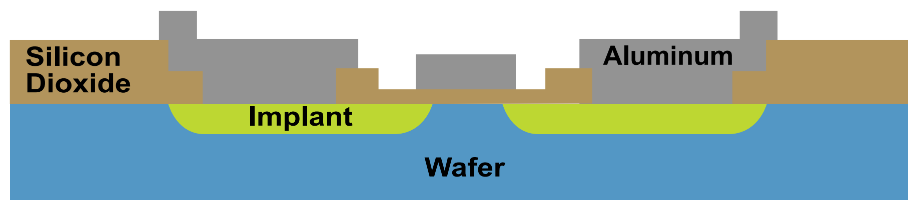
Methods:

1. Physical vapor deposition
2. Oxide growth
3. Chemical Vapor Deposition (CVD) – forms solid films on a wafer surface by chemical reactions of gaseous reactants at the wafer surface. During CVD, only the solid product is left as film and all other gaseous products are removed.

Types of CVD:

1. Atmospheric pressure chemical vapor deposition (APCVD)
2. Low pressure chemical vapor deposition (LPCVD)
3. Plasma-enhanced chemical vapor deposition (PECVD)
4. Photon or laser enhanced chemical vapor deposition (PHCVD of LCVD)

C. Metalization: A type of film deposition. Metalization is the deposition of a metal or metal alloy onto a wafer surface. This process is used to make IC interconnects, bonding pads, and diode (Schottky) junctions rectifying (to make an alternating current unidirectional) junctions. Schottky diodes are a two-terminal device that offers a high resistance to current flow in one direction and low resistance to current flow in the opposite direction. It is a lower voltage barrier than standard silicon diodes and is able to change operating states (on/off0 much faster than ordinary p-n junction diodes.



Metal Deposition

There are three methods in metalization:

1. Evaporation – The metal is evaporated with electrical thermal energy in an evacuated chamber (extremely low pressure). The metal vapor condenses on all surfaces including those exposed areas on the wafers.

2. Sputtering – Plasma energy is used to knock (sputter) fragments from the target allowing them to drift to the wafer surface and be deposited.

3. CVD – LPCVD is the most commonly used form of CVD for metalization. LPCVD provides better step coverage and better uniformity than the other methods of CVD.

Commonly used metals are aluminum, gold, platinum, titanium, and tungsten alloys.

Photolithography

This is the third major step in the process and allows for selective processing on the wafer surface. Photolithography defines the device or circuit on the wafer by using a mask (reticle) to transfer the IC design pattern onto the wafer. This transfer is similar to the development of a photograph. The wafer is covered with photoresist, a material that is light sensitive, and is soft baked to increase adhesion to the wafer.

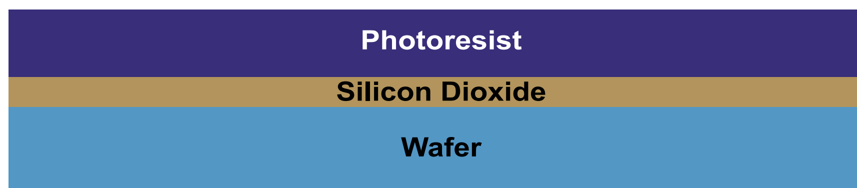
The photoresist is then exposed to light through the mask. There are two types of photoresists which have opposite effects when exposed to the light passing through the translucent regions of the mask. Positive photoresist will become softened, or solublized, to be rinsed away during the development stage leaving the unexposed hardened areas on the wafer. Negative photoresist will become hardened when exposed to light and the unexposed areas will be softened and be rinsed away from the wafer during the development stage. Positive photoresists usually form islands of photoresist while negative photoresist usually forms holes or "ditches."

Methods of exposure to light:

1. Contact printing – mask in contact with the wafer
2. Proximity printing – mask is close to wafer but does not come in contact with the wafer.
3. Projection printing – using mirrors to project the actual size image on the wafer.
4. Step and repeat – using high quality masks and image reduction lenses (5:1 or 10:1) to miniaturize the image. The wafer is sequentially moved until the entire wafer is exposed.

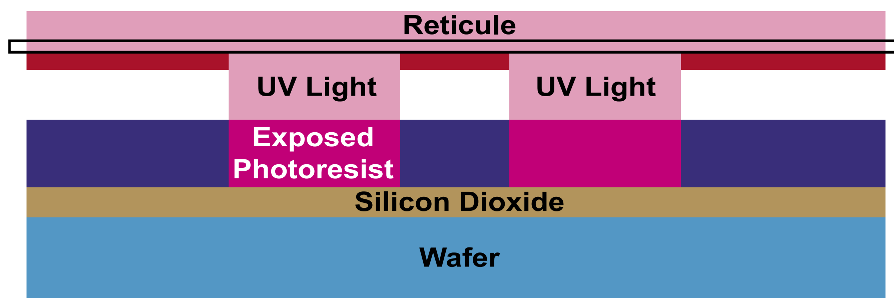
Major process steps:

1. Coating – surface prep
   photoresist application – negative = exposed areas harden
   – positive = exposed areas soluble
   – soft bake – increase adhesion



Photoresist Coating

2. Exposure – light passes through translucent areas of mask



Exposure

3. Developing – soluble portions of photoresist rinsed off.
4. Inspect

Etch Film

Etch is an intermediate process step used to remove material from the water surface. Removal may be patterned (in conjunction with photolithography) or unpatterned (taking place over the entire wafer surface). Both wet and dry etch involve three steps:

1. Disperse the etchant
2. Remove etched material
3. Remove the by-products created during etching

Wet Etch: uses acids, bases, and solvents that react with the wafer material to be removed. The etch chemicals change the exposed portion of the unwanted layer into a by-product by either oxidation/reduction reaction or an exchange reaction. The undercutting due to the isotropic etching imposes limits on critical geometries.

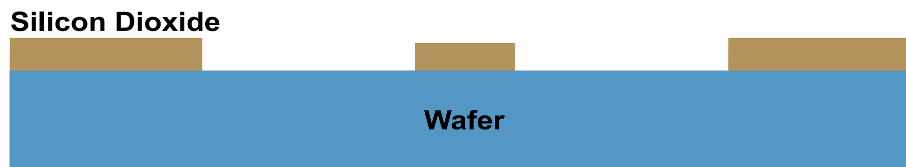
Dry (plasma) Etch: uses plasma to remove material by physical means, chemical reaction, or some combination of the two. Plasma is a mixture of charged and uncharged gas particles that maintain an overall electrical neutrality. It is an energetic, ionized gas sustained by RF energy (electromagnetic energy in the low kHz to low GHz radio frequency).

Three methods of dry etch:

1. Ion milling (sputter etch) – An entirely physical etching process using a plasma of non-reactive ions to physically remove material.

2. Plasma Etch – A chemical etching process using a plasma energy driven reactive gas rather than liquid chemicals.

3. Reactive ion etch – A dry etch process combining chemical and physical removal of wafer surface material.



Oxide Etch

Other Processes

1. **Diffusion:** Diffusion is the movement of particles from a region of high concentration to a region of low concentration. It is used to introduce dopants into the semiconductor wafer or films, and to cause dopants already present to migrate deeper into the substrate. High concentrations of dopant particles deposited on the surface of the wafer diffuse inward toward areas of low concentration. This diffusion of P-type and N-type dopants will modify the electrical characteristics of the silicon and produce the desired effect.

Diffusion is an intermediate step that may be repeated many times during the fabrication process. An entire wafer surface may be doped or just selected areas, in conjunction with photolithography and etch.

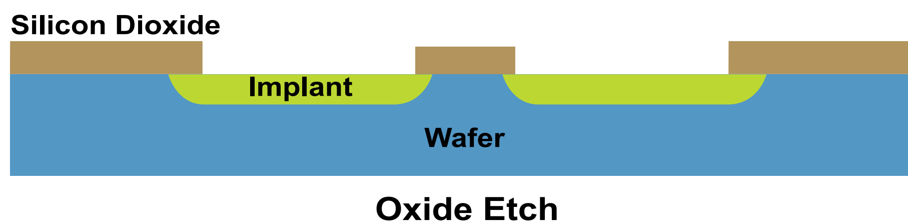
The diffusion process is dependent on time, temperature and the dopant species used. The depth of penetration of the dopant into the substrate is dependent on the oven temperature and the time of exposure. The diffusion process is a high temperature process that introduces dopant atoms into the semiconductor wafer or film as the result of sequential pre-deposition and thermal drive-in.

2. **Ion Implantation:** Ion implantation, like diffusion, is used to introduce dopant atoms into the substrate. This technique differs from diffusion in two respects:

   A. Ion Implantation processes at room temperature while diffusion processes at high temperatures.

   B. Ion Implantation peak dopant concentration lies below the surface rather than at the surface as in diffusion.

Ion implantation is used to modify the electrical characteristics of selected areas of the wafer. The ion implanter consists of an ion source, mass analyzer, accelerator, and a scanning system. The ion source (gun) is a chamber in which a selected gas is bombarded with electrons causing the removal (cation formation) or donation (anion formation) of electrons. An extraction electrode attracts the ions from the ion source and generates an ion beam separating out the required ion in the mass analyzer. The mass analyzer is basically an electromagnet (mass spectrometer) which separates ions based on the charge-to-mass ration. When ions pass through the magnetic field in the mass analyzer the heavier atoms travel in a wider arc than the lighter ions. The desired ion can be selected by setting the strength of the magnetic field. The desired ions are accelerated to the required energy by a series of high voltage electrodes called an accelerator. The resultant ion beam is focused using an electrostatic and magnetic quadruples.



Oxide Etch

Ion implantation bombardment of the crystal by ions damages the crystal lattice structure. The regular ordered pattern of the lattice is disrupted and the implanted ions are not located in the lattice. Annealing restores the crystal lattice structure and incorporates the implanted ions into the lattice thereby activating them. Annealing is exposing the implanted wafers to a high temperature (1000ºC) thermal cycle.

Fabrication of the wafer is now complete. The individual devices on the wafer are electrically tested and separated to then be assembled into a final product.

Wafer-Probe Test

The purpose of this test is to gain information of process yields and final performances. Any individual devices that do not pass this test are rejected and not assembled. Good devices (die) are used to assemble the final product.

Assembly

The purpose of assembly is to package the die in a form that is usable to the customer and to protect the quality of the device. The following is a list of steps in the assembly process:

1. Die (chips) separation with diamond saw.
2. Mounting process – places die onto lead frame strips.
3. Wire bonding – a computer controlled process in which gold or aluminum wires from the pads on the die are attached to the inner leads on the lead frame. These wires connect the die (chip) integrated circuit to the outside world.
4. Encapsulation – Die is covered or enclosed with a plastic coating using epoxy to seal.
5. Symbolization – A laser writes the part, lot number, date, and country of origin on the package for identification.
6. Trim and form the leads.
7. Solder tin leads and rinse.

Final Test

This final step in the manufacturing process is a series of AC and DC measurements of the performance of the die. This test is analogous to revving your car engine under many different environmental conditions to insure it will perform correctly. This is the last check for device quality before the package is shipped to the customer.

Glossary

amorphous	Without any definite shape.
atomic structure	Arrangement of protons, neutrons and electrons in the atom.
bipolar	The family of solid-state devices whose operation depends on the conduction of two polarities of charge carriers.
bonding spots	Spot for bonding wires to the device
capacitor	A discrete device which stores electrical charge on two conductors separated by a dielectric.
ceramic	A material used in manufacturing packaging made essentially from a nonmetallic mineral by firing at high temperatures (porcelain, glass, vitreous enamels).
chip	Die or device, one of the individual integrated circuits or discrete devices on a wafer.
cmos	(complimentary field-effect transistor) N- and P-channel transistor on the same chip.
covalent bonding	A type of strong chemical bonding involving the sharing of valence electrons between atoms to complete their valence shells.
crystalline	Having the regular internal arrangement of atoms, ions, or molecules characteristic of crystal.
die	Chip or device, one of the individual integrated circuits or discrete devices on a wafer.
dielectric	The material used in solid-state devices to electrically isolate particular elements.
diffusion	A process that introduces minute amounts of impurities into the a substrate material (silicon) and allows the impurity to spread into the substrate. Time and temperature dependent process.
diode	A device which enables current flow in one direction only.
doping	The introduction of an impurity into the crystal lattice of a semiconductor to alter its electronic properties.
electron	A charged particle revolving around the nucleus of an atom. It can form bonds with electrons from other atoms r be gained or lost to form ions.
epoxy	A flexible usually thermosetting resin made by polymerization of an epoxide and used chiefly in coatings and adhesives.

ingot	A mass of silicon crystal grown to a convenient shape for storage, or transport for processing at a later time.
insulator	A material that is a poor conductor of electricity. Can be used for separating or supporting conductors to prevent an undesired flow of electricity.
integrated circuit	A tiny complex of electronic components and their connections that is produced on a small slice of silicon material (wafer).
interconnects	Electrical conductors between layers that connect devices to form the IC circuitry.
ionization	When an atom gains electrons to become negatively charged or loses electrons to become positively charged.
Isotropic	The same in all directions; an isotropic etch etches vertically and horizontally at the same rate.
lattice structure	An orderly pattern of atoms.
leads	A metal strip on the wafer surface.
miller index planes	Crystal lattice orientations based on the angles created by the unit cells.
N-type	A semiconductor material in which the majority of carriers are electrons and therefore negative. These dopants in silicon are group 15 elements, in which the fifth outer electron is free to conduct current.
P-type	Semiconductor material in which the majority of carriers are holes and positive. These dopants in silicon are group 13 elements.
polycrystalline	Heterogeneous crystal orientation, no specific internal arrangement.
quadrupole	A system composed of two dipoles of equal but oppositely directed moment.
rectifying junctions	To make an alternating current unidirectional
resistance	The opposition offered by a substance to the passage through it of a steady electric current.
resistor	A device that has electrical resistance and is used in an electric circuit for protection, operation, or current control.
RF energy	(Electromagnetic energy in the low kHz to low GHz - radiofrequency).
semiconductor	An element such as silicon or germanium, intermediate in electrical conductivity between the conductors and the insulators.

Schottky diodes A two-terminal device that offers a high resistance to current flow in one direction and low resistance to current flow in the opposite direction. It is a lower voltage barrier than standard silicon diodes and is able to change operating states (on/off) much faster than ordinary p-n junction diodes.

soild-state devices Designation used to describe devices and circuits fabricated from solid materials such as semiconductors or thin films from devices and circuits using electron tube technology.

transistor A semiconductor device that uses a stream of charged carriers to produce active electronic effects.

thin Films Metals, semiconductors, or insulators used as a protective layer, or to construct a circuit or device components.

unit cells The group of atoms in a crystal that is repeated in three dimensions in the crystal lattice.

wafer A thin, round slice of semiconductor material, from which the chips are made.

SEMICONDUCTOR SCIENCE

Name ______________
Date ______________
Class ______________

Chemistry Student Activity 1
Density of Solids

Introduction
All matter is made out of atoms. Density is a physical property of matter which depends on both the type of atoms forming the substance and the arrangement of these atoms . In this activity, you will experimentally determine the density of both silicon (Si) and quartz (SiO_2) and investigate the atomic structure of both solids.

Objective: To experimentally correlate the molecular structures of silicon and quartz to their respective densities.

Materials
Safety goggles
8 100-ml glass graduate cylinders
Metric balances
Tap water
8 electronic grade Silicon fragments, approx. 2 cm. in diameter
8 quartz fragments, approx. 2 cm in diameter

Density Determination by Water Displacement

Procedures

1. Obtain samples of silicon and quartz. Make sure that the samples are clean and dry and that you can distinguish between them. Obtain the mass of each sample to the nearest 0.01 gram using the metric balance. Record the mass of each sample in a data table.

2. To find the volume of each sample, fill a 100-ml graduated cylinder approximately half way full with tap water. Record the volume of water in the cylinder. Tilt the cylinder and slide one of the dry samples carefully into the water to avoid breaking the graduate cylinder or splashing the water. The entire sample must be under water or you will have to begin the procedure again using a larger volume of water. Record the final volume of the water containing the submerged sample.

Table 1.1 Data and Calculations

	Si				SiO_2			
	1st trial	2nd trial	3rd trial	Average	1st trial	2nd trial	3rd trial	Average
Mass of Sample(g)								
Initial volume of water(ml)								
Volume of water+ sample(ml)								
Volume of sample(ml)								
Density of sample(g/ml)								

Analysis Questions:

1. Now examine and compare the piece of silicon as well as the piece of quartz. What do you think determines the experimental differences in densities between these two solid substances?

   ____
   ____
   ____

2. Use your periodic table to look at the atomic mass and atomic number for Silicon and Oxygen. Silicon metal is a solid made of single atoms of silicon, whereas quartz is made of both silicon and oxygen. Why do you think their densities differ?

   ____
   ____
   ____

3. Bonus question: Why are silicon atoms larger in size than oxygen atoms? Hint: Look at the periodic table of elements and draw the atomic structure of oxygen and silicon.

   ____
   ____
   ____

SEMICONDUCTOR SCIENCE

Name ____________________
Date ____________________
Class ____________________

Chemistry Enrichment Activity
Density of Solids

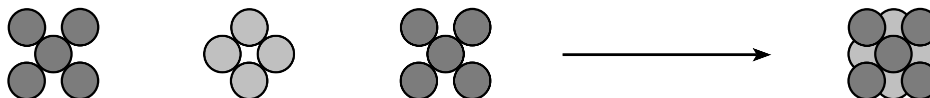
Introduction
All matter is made out of atoms. Density is a physical property of matter which depends on both the type of atoms forming the substance and the arrangement of these atoms . In this activity, you will build and compare the crystal structure of Silicon (a face centered cube) to the hexagonal structure of quartz

Materials: 1” Styrofoam balls
1.5” Styrofoam balls
Toothpicks

Part 1: Build a simple molecular model of Silicon

Procedures

1. Use toothpicks to create the three layers as shown in the figure below. Connect the larger one and a half-inch Styrofoam spheres by using toothpicks.



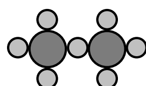
2. Place the first layer (A) on the lab table. Now place the second layer (B) over the first layer so that the four spheres of layer B rest in the spaces between the corner spheres of layer A.

3. Finally, place the third layer (C), over layer B in such a way that the spheres of layer C are directly over the spheres of layer A. Study this model carefully and try to explain why this type of crystal is called **face-centered cubic**.

Part 2: Build a simple molecular model of Quartz

Procedures:

1. Using the same procedure, build a silicon dioxide tetrahedron (see picture below.) The 1.5” spheres represent the atoms of silicon and the 1” spheres represent the atoms of oxygen.



Analysis Questions:

1. Compare the face centered cubic structure of silicon with the hexagonal crystal structure of quartz. Do you think that the arrangement of atoms alone influences the density of the crystals? Explain.

   ____
   ____
   ____
   ____
   ____
   ____

2. If your model of quartz was built only of silicon atoms, would that change your answer to question number one? Explain.

   ____
   ____
   ____
   ____
   ____
   ____

SEMICONDUCTOR SCIENCE

Name ______________________
Date ______________________
Class ______________________

Chemistry Activity 2
Doping by Diffusion

Introduction
Industry and technology use many scientific principles and phenomena and apply them in useful ways to manufacture complex electronic devices. Many of us use these devices without even thinking about what they are made of or how they work. Some of these devices include the microchips (the brains) of computers, watches, beepers, electronic video game machines, and cellular phones.

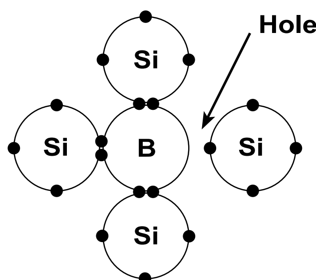
Objectives: To simulate the process of semiconductor doping.

To compare a lab model of diffusion to the process of doping used in manufacturing of silicon wafers.

Materials:
Beads
Index cards
Scissors
Template for doping simulation

Part 1: Doping
Doping is the addition of atoms to a silicon wafer in order to change the conductivity of the silicon. Pure silicon does not conduct electricity. By adding atoms of Phosphorus an n-type wafer is produced, when boron atoms are added, a p-type wafer is produced. There are differences in the electrical properties of these wafers. The layering of p or n- type silicon on a wafer leads to the formation of different electronic components such as transistors, diodes, integrated circuits, the stuff that makes your beeper or computer work!

A. P-type Silicon
Atoms of boron are used to "dope" or change the conductive properties of the silicon wafer. The end result is that the boron atoms penetrate the wafer and four silicon atoms surround each one. Since boron is a member of family 3A in the periodic table, it has 3 electrons in its valence shell. When surrounded by 4 silicon atoms it forms covalent bonding with three of the silicon atoms, but there is a "hole" because of the lack of bonding right at the site between the fourth silicon atom and the boron. This hole is readily available for an electron coming from a current flow to jump in. Boron creates a P (for positive) type material. Look at the bonding model diagram below to understand the formation of the p-type silicon.



What is the chemical formula for this p-type Silicon?

____

B. N-type Silicon

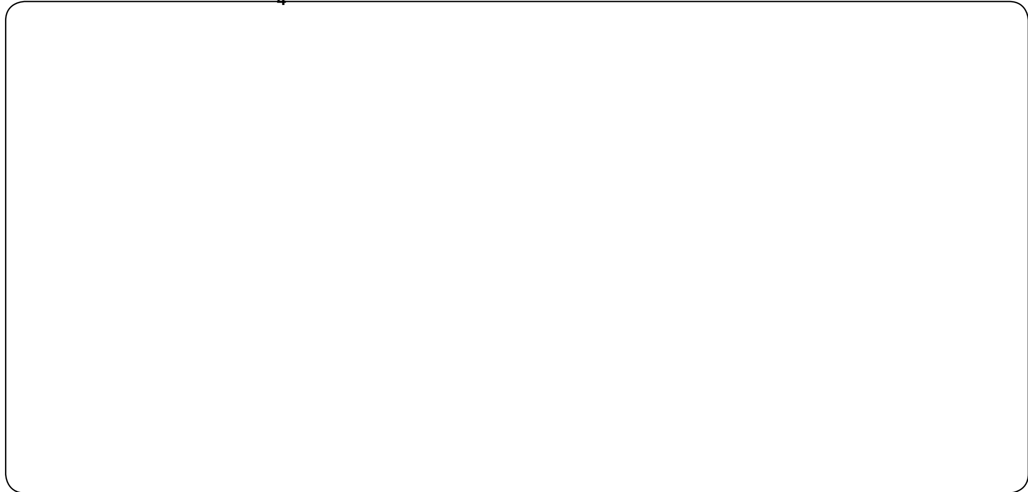
This type of Silicon is usually doped with phosphorus (P) or arsenic (As). Both of these elements belong to family V of the periodic table.

How many valence electrons do these elements have?

As the silicon wafer is doped with the impurity atoms of phosphorus or arsenic atoms penetrate the wafer and four silicon atoms surround each one.

Using the example of the doping with boron as a model, draw the bonding model diagram for the n-type Silicon in the space below.

The formula is $AsSi_4^{-1}$.



C. Model the Electron flow between the p-type and n-type silicon

Procedures:

1. Use the templates of silicon and boron atoms to construct a model of the p-type material by placing the boron atom in the middle and surrounding it with the four silicon atoms. Your templates model should resemble the bonding model diagrams.Use the beads to represent valence electrons.

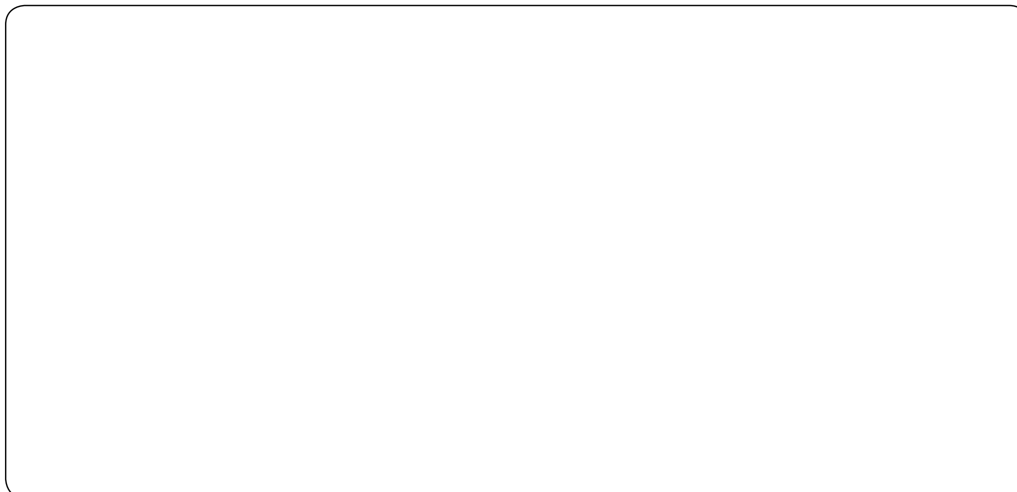
2. Use the phosphorus atom template plus another set of four silicon templates to prepare a model of the n-type silicon.

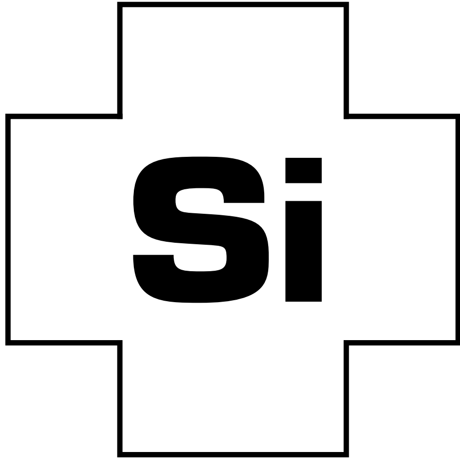
3. Place the models of the p-type and the n-type silicon side by side.

4. Take a free electron bead from one of the silicon cards surrounding the phosphorus atom card and figure out how this electron will move from the n-type material to the p-type material.

   If these two pieces of doped silicon (p-type and n-type) are electrically connected by a circuit, which way will the electrons in the silicon flow?

5. In the space below, prepare a diagram that shows the electron flow as demonstrated by your atom template activity.

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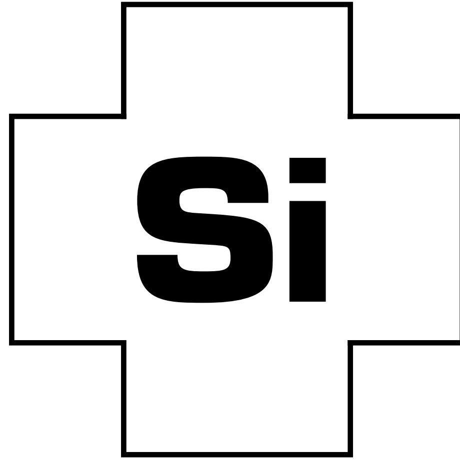
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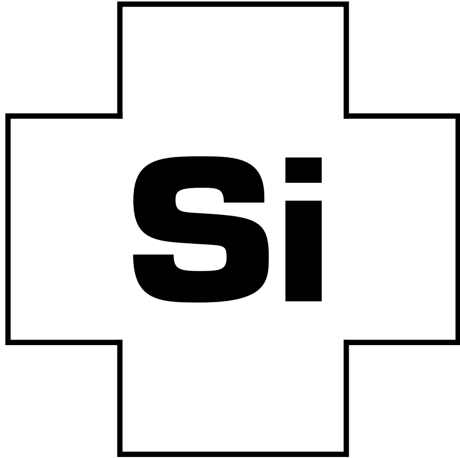
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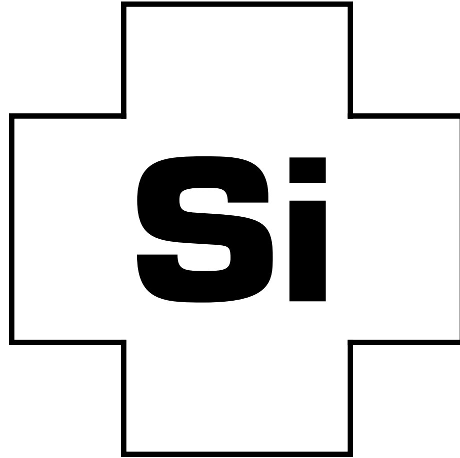
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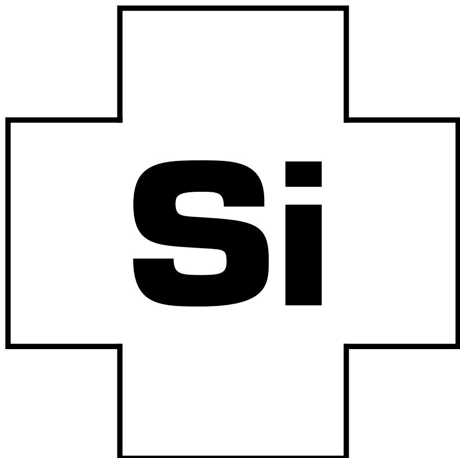
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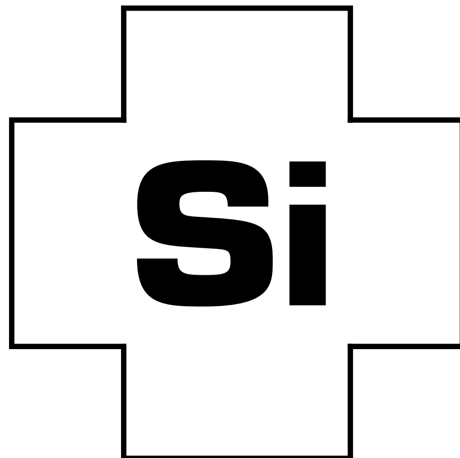
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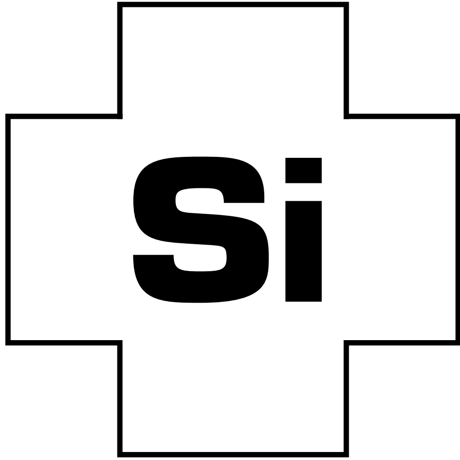
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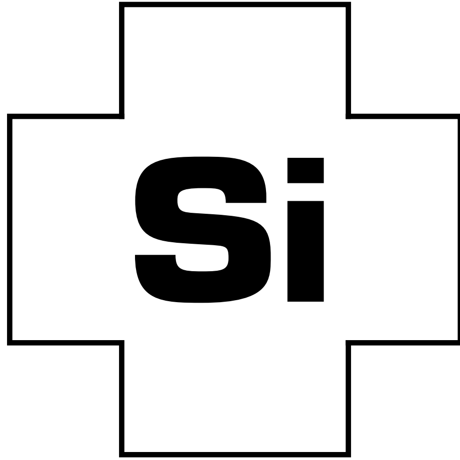
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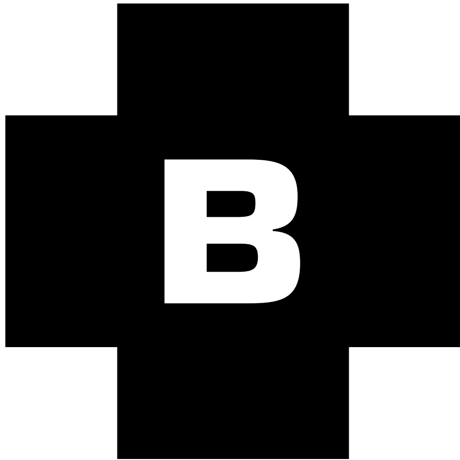
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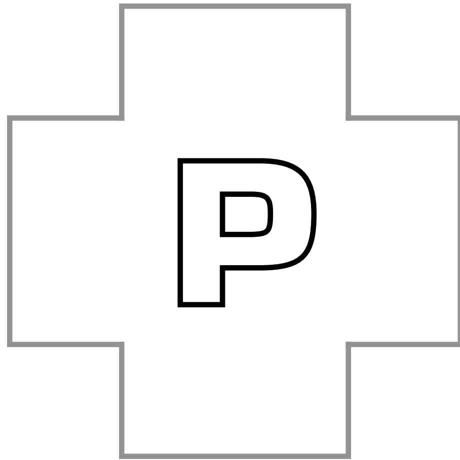
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Chemistry Activity 3
Doping by Diffusion

Introduction
The process of diffusion involves the random motion of gaseous particles (the atoms or molecules of a gas) from an area of high concentration to a region of low concentration. In the semiconductor industry scientists take advantage of diffusion to dope or introduce atoms into a pure silicon wafer to change its conductive properties. Some of the compounds used in dopant diffusion are: BCl_3 (boron trichloride), PH_3 (phosphine), and AsH_3(arsine).

Objectives: To simulate the process of semiconductor doping.

To compare a lab model of diffusion to the process of doping used in manufacturing of silicon wafers.

Materials:
Petri dish with gelatin
Clear plastic resealable bag
Dropper bottle of ammonia
Piece of white paper

Procedures:

1. Place the uncovered Petri dish inside the clear resealable baggie. Place the lid inside the baggie.

2. Place two droppers full of ammonia in the lid of the Petri dish. Seal the bag. Allow for diffusion to take place for three minutes or until you no longer see changes in the gelatin.

3. Place a piece of white paper on the lab table.

4. Carefully observe the petri dish. Record your observations. Remove the Petri dish from the baggie and measure the depth of diffusion in millimeters.

5. Measure the thickness of the gelatin layer in millimeters. Calculate the percent diffusion.

   $$\text{Percent Diffusion} = \frac{\text{Thickness of the Diffusion Layer}}{\text{Thickness of the gelatin}} \times 100$$

   Percent Diffusion =

6. Wash the baggie and the petri dish lid with soap and tap water. Rinse them with distilled water and dry them with a paper towel. Wash your hands

Analysis Questions:

1. What did you observe on the petri dish after placing the beaker with ammonia under the large beaker?

2. How was this experiment similar to the doping of silicon wafers with boron or arsenic atoms?

3. What would you do to speed up the diffusion process observed in this experiment?

4. How deep did the ammonia penetrate into the gelatin? How can you tell?

5. Why didn't the ammonia diffuse all the way into the gelatin? Please be specific and use scientific terms.

6. Dopants diffuse into 0.5 mm silicon wafers to an average depth of 3.44×10^{-3} cm. Calculate the percentage of the wafer that is doped.

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Chemistry Activity 4
Etching and Photolitography

Introduction
Manufacturing the microchips that run devices such as computers, calculators, beepers, and watches requires many steps. One of the steps that enables electronic devices to be built on silicon wafers is etching. Etching is the removal of a material in specified areas through a wet or dry chemical reaction. Before etching can take place, an electrical engineer designs a circuit based on specifications from the product manufacturer. This circuit design is printed onto the silicon wafer using a process called photolithography. In this activity you will simulate the processes of photolithography and etching.

Objectives: To relate prior knowledge of chemical reactions to the process of making microchips.

To simulate photolithography and etching and understand the chemical and physical principles involved.

Materials:

- Safety goggles
- Lab apron
- Candle or wax crayon
- 0.5 mm thick galvanized steel plate or other galvanized metal
- Molar solution of $Cu(NO_3)_2$
- Circuit pattern transparency film
- Blueprint paper
- Dropper bottle of household ammonia
- Petri dish
- Masking Tape
- Pencil
- Wash bottle of distilled deionized water

Part 1: Developing a Photolithography Mask
During this step, you will simulate the photolithography process of wafer fabrication. The actual process of building a microchip requires the precise alignment of up to 58 different photolithography masks. The end result is a complex integrated circuit, which performs the “thinking tasks” of an electronic device.

Procedures:

1. Obtain a piece of blueprint paper from your teacher. Be careful not to expose the yellow, photosensitive side of the paper to light. Keep the blueprint paper in the protective bag until you are ready for step 2.

2. Take the piece of blueprint paper out of the bag and carefully place and tape the circuit mask (printed transparency film) over the yellow side of the blueprint paper. The dark pattern on the mask is an enlarged section of an actual circuit used in microchips.

3. Expose the paper with the fastened transparency film to sunlight for enough time to cause the blueprint paper to turn white. Do not remove the mask!

4. The blueprint paper will be developed in a petri dish. Trim the blueprint paper to the right size by cutting along the outside of the outer circle printed on the mask.

5. Place a piece of double-sided tape on the non-photosensitive side of the blueprint paper. Separate the blueprint paper from the mask.

6. Add four droppers full (four mls) of household ammonia into a Petri dish. Your teacher may already have the developing dishes ready to go under the fume hood

7. Use tape to attach the blueprint paper to the inside of the Petri dish lid. Place the lid on the Petri dish. Do not allow the ammonia solution to make direct contact with the blueprint paper. Wait about 3 minutes.

8. Open the Petri dish and remove the blueprint paper.

9. Put the lid back on the Petri dish and follow your teacher's instructions for disposal of the ammonia solution.

10. Compare the pattern transferred to the blueprint paper to the original mask. Wash your hands

Part 2: Etching

Photolithography transfers the circuit design on the mask to a layer of photoresist, which is placed on the wafer prior to each etching cycle. Once the photoresist has been developed, some areas of the wafer will "resist" chemical reactions while others won't. This allows etching to permanently transfer the mask pattern into the surface layer of the wafer. After etching, a layer of oxide is deposited on the silicon wafer and another round of photolithography and etching can begin, building the microchip layer by layer. The layers are connected with aluminum or copper wires, or "interconnects".

You will now use the mask developed in step one to etch a piece of galvanized metal.

Procedures:

1. Prepare the galvanized metal plate by polishing it thoroughly on one side with a piece of steel wool. The metal surface should be shiny and uniform in appearance.

2. Cover the polished side of the plate with a layer of wax by rubbing the end of a candle over it or coloring it with a crayon. This step simulates the application of the photoresist layer.

3. Place the blueprint paper, developed side up, on top of the waxed steel plate.

4. Trace the circuit on the blueprint paper with a sharpened No. 2 pencil. Press down hard enough to remove the wax from the plate (the wax sticks to the back of the blueprint paper wherever pressure is applied).

5. Peel the blueprint paper off of the metal plate.

6. Use the tip of your pencil to remove any traces of excess wax from the circuit design on the steel plate.

7. Cover your lab table with thee layers of paper towels, and then place the steel plate pattern side up on them.

8. Cover the circuit design on the metal plate with 0.5 Molar solution of $Cu(NO_3)_2$.

9. Leave the solution on the plate for approximately five minutes.

10. Use the wash bottle to rinse the copper solution off of the plate and into a beaker.

11. Blot the plate dry with a paper towel.

12. Carefully remove the rest of the wax from the plate with steel wool. Do not worry if you scrub over the etched circuit pattern. If time permits repeat the process of etching two more times using different masks to complete the entire circuit design.

13. Follow your teacher's instructions for disposal of all waste materials.

Analysis Questions:

1. The width of a line on the circuit section you etched onto the galvanized plate is roughly 0.25mm.The actual width of a circuit line on an 80 mm^2 silicon microchip is 0.25 microns (2.5×10^{-7}m) or the equivalent to 1/400 the length of a human hair. Now assume that you have been assigned as a project to build a model of a microchip. Calculate to scale the relative size of your "microchip" assuming your line size of 0.25 mm.

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2. Galvanizing is a process used to protect a metal from corrosion. The metal in need of protection from rusting is coated with a more reactive metal such as zinc. Essentially the galvanizing metal is sacrificed to protect the less reactive metal. Write a balanced chemical reaction that illustrates the etching reaction you performed on part two of the lab.

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3. What type of reaction is it? Write the net ionic equation for the reaction.

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4. Was there a residue other than wax during the final polishing / If so, what was it?

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5. Can you think of another chemical reaction that could be used to etch silicon or aluminum or copper?

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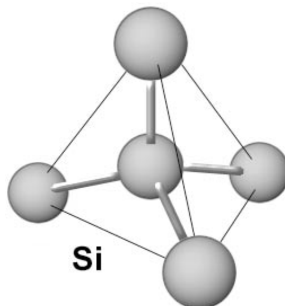
Chemistry Activity 5
Crystals

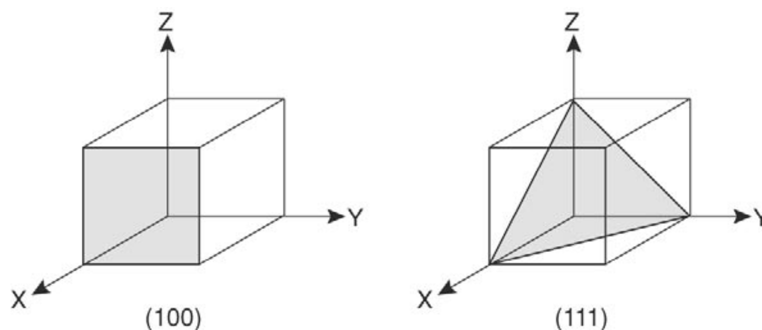
Introduction
Silicon is in the group IV, the carbon family, and has four valence electrons which can be shared with four other atoms to form four covalent bonds. By sharing electrons this way each atom's valence shell is complete, resulting in solid matter that is electrically stable and a poor conductor. The four electron pairs in the covalent bond will exhibit shell electron pair repulsion producing a tetrahedral molecular geometry.



Solids are arranged in crystalline or amorphous forms. The degree of organization determines the form the finished material will take. Plastics and glass are good examples of amorphous structures and represent a material without a definite periodic arrangement of their atoms. Semiconductors and metals are examples of crystalline materials in which the atoms occupy definite positions with respect to one another.

There are two levels of atomic organization for crystal structures. The individual atoms organizational structure is called the unit cell and is characterized by atoms arranging themselves at specific points in their structure. This unit cell repeats itself throughout the structure forming a lattice. One silicon atom covalently bonded with four other silicon atom forms the tetrahedral structure called a bonding unit. The unit cell of silicon consists of eight bonding units that form the basis for a crystal lattice.

The lattice is a repetition of unit cells and when viewed from different angles or planes will give different geometries or patterns. These different geometries are called Miller Index Planes and are the second level or organization in crystal structure. They describe the orientation of the crystal, which is dependent on the orientation of the individual unit cells within the crystal.



In the semiconductor industry the orientation of crystal is crucial to performance. As the ingot is cut to produce wafers the planes resulting for the slices must have identical planes. Each type of plane is unique, differing in atom count and binding energies and therefore in chemical, electrical and physical properties. The specific plane must be the same for the entire wafer to insure consistency of performance for any circuits produced on that wafer. The two most common Miller indices are 100 and 111 are shown below: Semiconductor wafers are cut from large crystals of semiconductor material called ingots. The process of converting the single crystal into a large single crystal ingot with the correct orientation is called crystal growing.

The most common method of crystal growing is called the Czochralski (CZ) method. In this method the crucible is filled with polysilicon chunks of a variety of orientations and heated to a molten state. A small seed crystal of the correct orientation (<100> or <111>) is positioned just above the molten silicon (melt). The seed crystal is slowly raised above the melt and the surface tension between the seed and the melt cause a thin film of the melt to adhere to the seed and cool. As it cools the atoms of the melted silicon orient themselves to the same Miller indices plane crystal structure as the seed crystal. The net effect is the crystal orientation of the seed is propagated in the growing crystal and eventually into the entire large crystal (ingot) from which the wafers are cut.

Objectives: Build and describe the shape of a covalently bonded pure silicon molecule using the valence shell electron pair repulsion theory.

Build the structures representing the 2 types of Miller index planes used in the semiconductor industry.

Combine the individual unit structures and describe how a seed crystal determines the crystal lattice of an entire ingot.

Materials: Molecular model kits with carbon atoms used for silicon.
20 centicubes (1cm^3 plastic interlocking cubes)

Procedures

1. Form lab groups of four. Send two people to the center lab station to get the materials needed to do this activity.

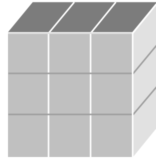
2. Each pair in the lab group picks up a silicon atom and places four sticks, each representing a bonding site, in the atom oriented so that the sticks are as far away from each other as possible (angle of 109.5^o).

3. Now place a silicon atom on each bonding site so that four silicon atoms are bonding with the central silicon atom. This structure represents tetrahedral molecular geometry and demonstrates the 3-dimensional shape of the Si molecule also known as a silicon tetrahedral bonding unit.

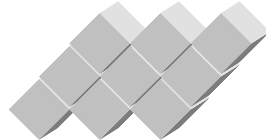
4. Using the bonding units, atoms, and sticks from step 3 have one pair of lab partners make a Miller indices 100 plane and the other pair make a Miller indices 111 plane for your lab group. (Refer to the diagrams at your lab station for the structure)

5. If eight of these bonding units were placed together you would have a silicon unit cell which is represented by a centicube. The orientation of this unit cell would be determined by the Miller indices plane you made in step 4.

6. If your lab pair made the Miller 100 plane then interlocked 9 cubes together so that they are flat on top it may look like this:



7. If your lab pair made the Miller 111 plane by interlocking 9 cubes together so they are triangular shape on top it may look like this:



8. What you have made so far would represent a single crystal of either Miller indices 100 or 111 plane. Look around the lab at different lab groups and, when directed to by your instructor, experiment how you could form a much larger crystal. (Find another group, or many groups) and demonstrate what happens as unit cells overlap to form the larger crystal structure. Remember when combining your individual crystals you must retain the Miller indices of either 100 or 111 for the plane of the larger crystal ingot.

Some questions to be considered by your lab group:

1. What effect does crystal orientation have on the silicon crystal?
2. What is the melting point of solid polycrystalline silicon?
3. Why do we melt the polycrystalline silicon down to a homogenous liquid?
4. Which orientation would you select for your seed crystal? and (explain the effect your choice will have on the finished wafer.)

Analysis Questions:

1. Diagram the structure of an atom and describe the electrons, protons, and neutrons.

2. State the relationship between the location of an element on the periodic table and the number of electrons in the valence shell.

3. Diagram and describe the shape of a covalently bonded pure silicon molecule using the valence shell electron pair repulsion theory.

4. Diagram and describe the structures representing the 2 types of Miller index planes used in the semiconductor industry. How does the semiconductor industry take advantage of the two different types of orientations?

5. Diagram how the individual unit structures are combined to form the larger crystal and describe how a seed crystal determines the crystal lattice of an entire silicon ingot.