NACK NETWORK

Building College-University
Partnerships for Nanotechnology
Workforce Development

How is Nanotechnology Changing the Electronics Industry?

Welcome to NACK's Webinar

Today's Presenter

Center for Nanotechnology Applications and Career Knowledge (NACK)

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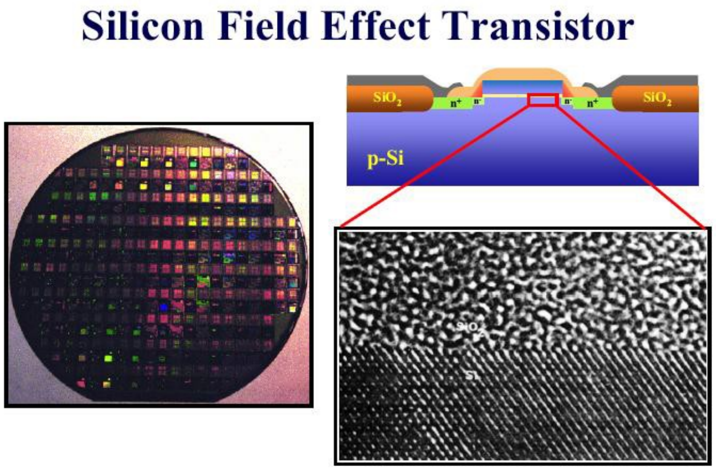
Miniaturization in Microelectronics



MOSFET = Metal-Oxide-Semiconductor Field Effect Transistor

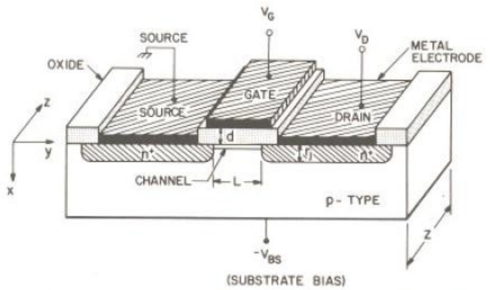
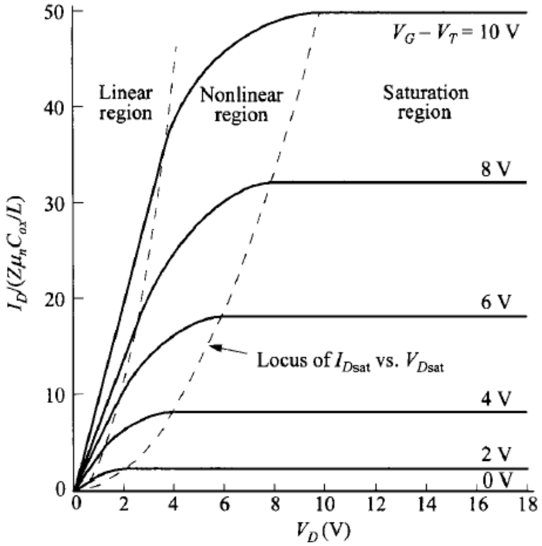
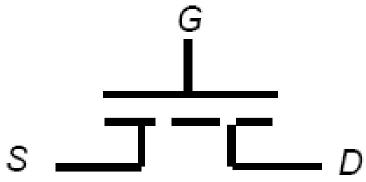
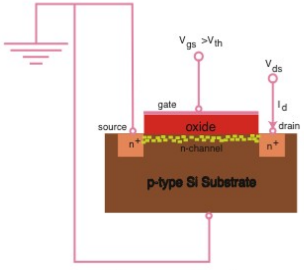


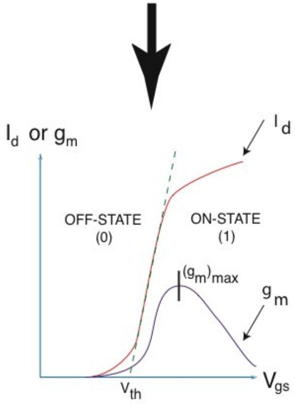
Fig. 3 Schematic diagram of a MOSFET. (After Kahng and Atalla, Ref. 4.)





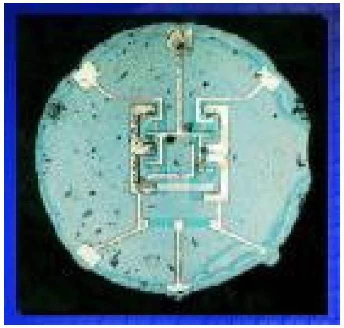


Common Biasing

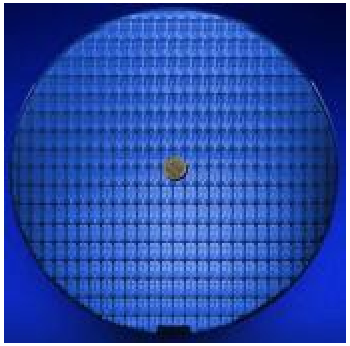


IV Output

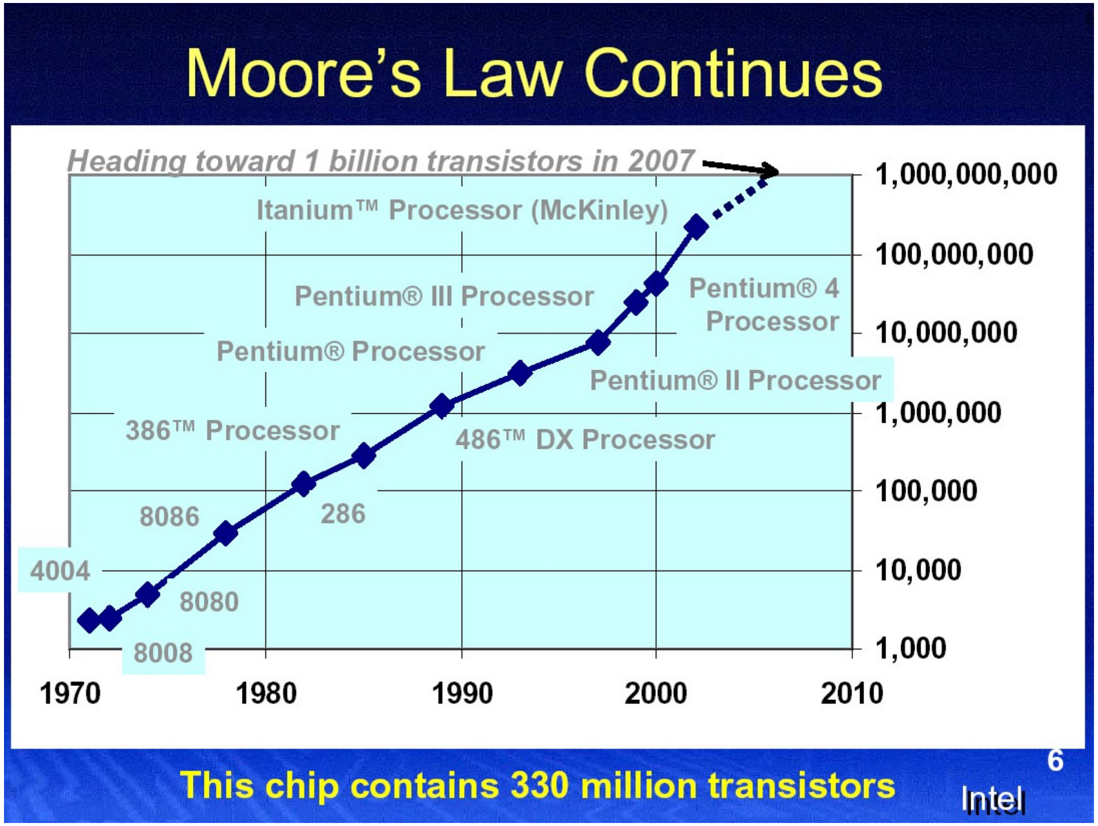
"Physics of Semiconductor Devices", S.M. Sze, John Wiley & Songs publishing, 1981



1961 *The first planar integrated circuit (IC)*



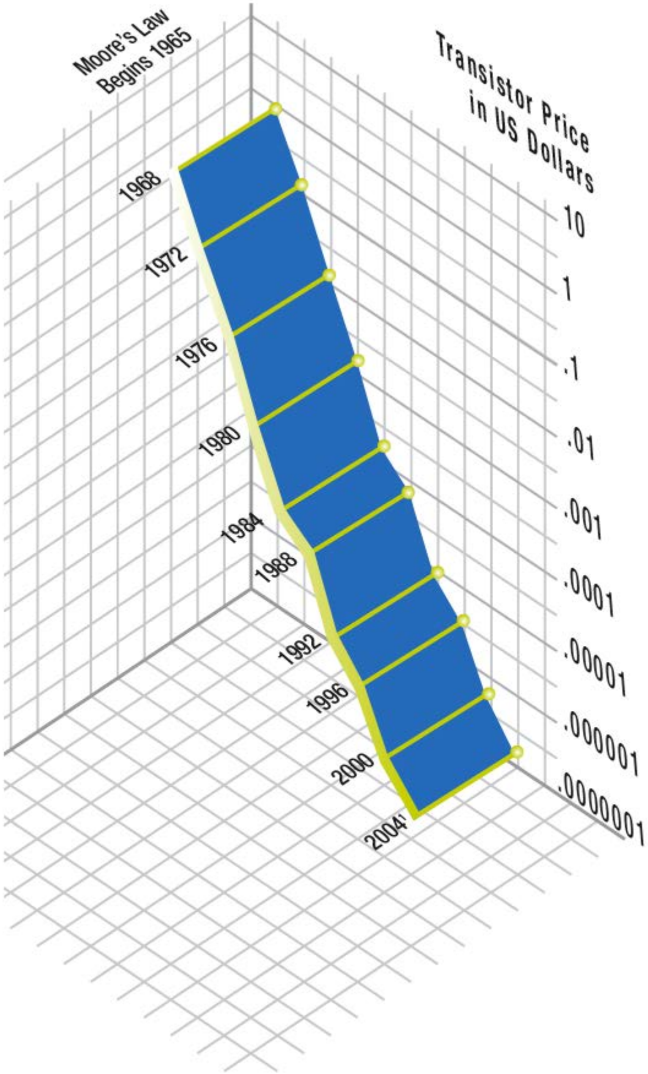
300 mm wafer



Source : Bob Trew, NCSU

1965 *"Cramming more components onto integrated circuits" by Intel Co-Founder Gordon Moore.*

Moore’s Law (continued)

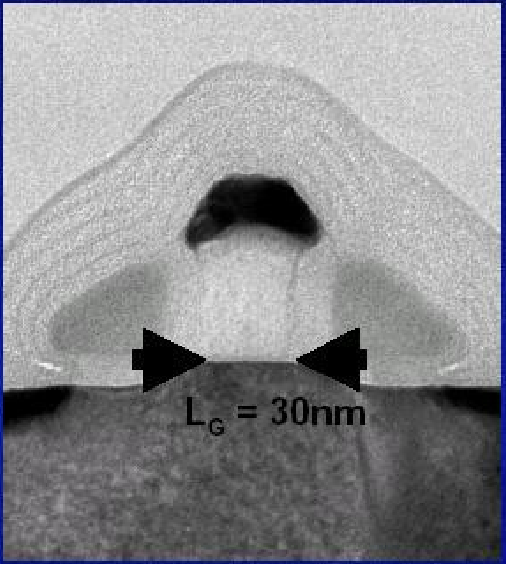


ftp://download.intel.com/museum/Moores_Law/Printed_Materials/Moores_Law_2pg.pdf

Intel's Transistors Keep Shrinking

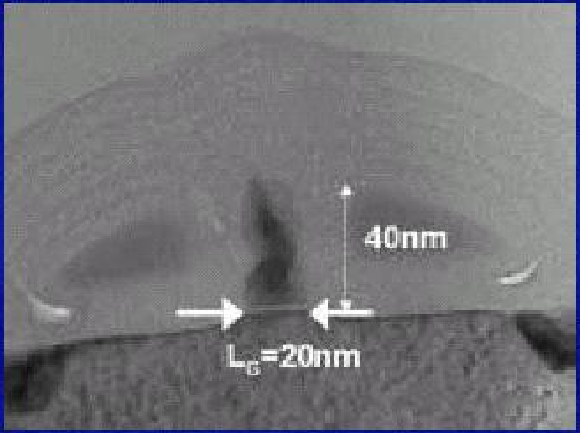
Record small transistors produced in Intel Labs

30 nm



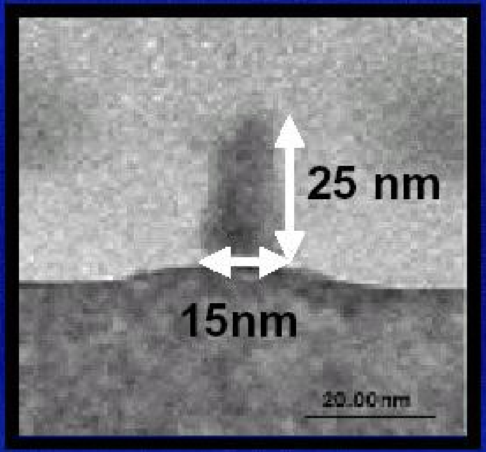
December 2000

20 nm



June 2001

15 nm



Today

Source : Bob Trew, NCSU

Intel Labs

Why is Nanotechnology important to Microelectronics?*

- The “push” in microelectronics is constantly toward smaller transistors. This allows faster and more devices on a chip giving more memory and more functionality; i.e., giving new products to sell.
- The microelectronics industry has reached more than a billion transistors on a chip! Transistors in production are smaller than 45nm!
- Today’s advanced devices require that the microelectronics industry uses nanotechnology everyday to make these transistors.

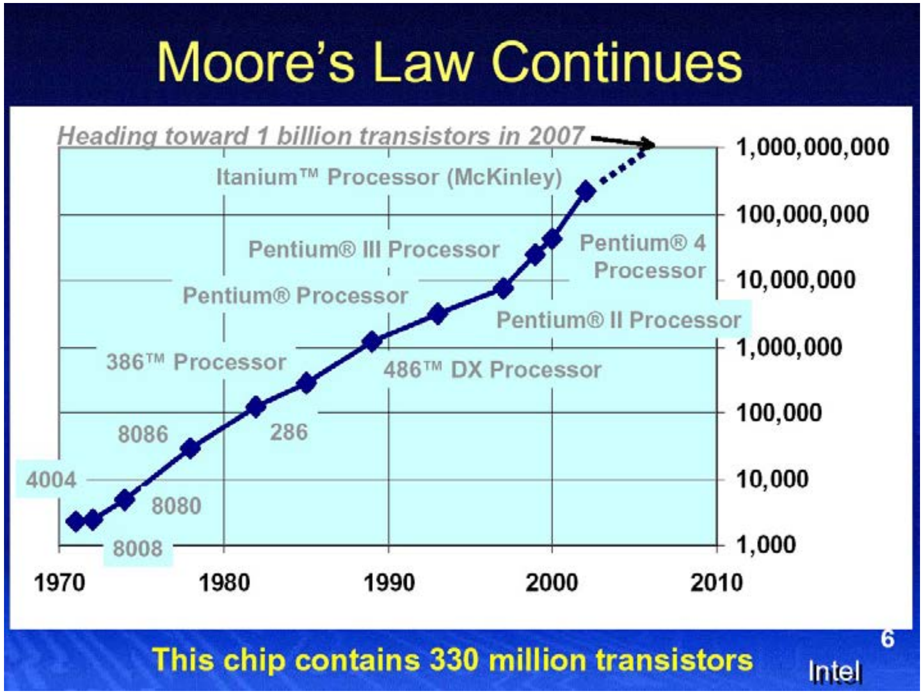
**Source : S. J. Fonash, class notes, Penn State University*

Why is Nanotechnology important to Microelectronics? (ctd.)*

- According to Dr. Andrew Moore (a founder of Intel) the number of transistors on a chip doubles about every 18 months.

- This observation is known as Moore’s Law.

- It captures the speed with which microelectronics companies have been pushing each other to smaller and smaller transistors.



Source : Bob Trew, NCSU

Why is Nanotechnology important to Microelectronics? (ctd.)*

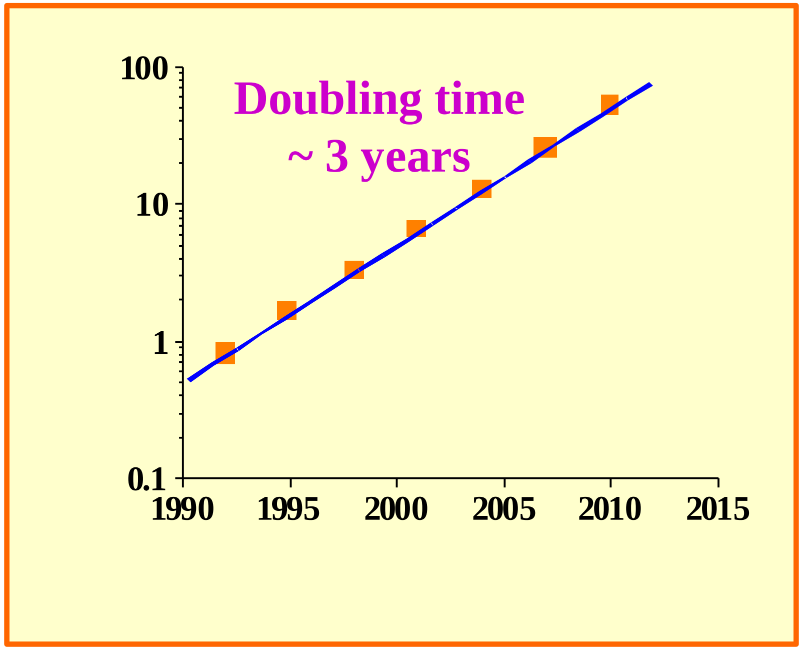
- The microelectronics industry is using top-down nanofabrication to make its nano-scale advanced transistors.
- All the deposition, lithography, material modification, and etching steps required by top-down fabrication mean cleanrooms and very expensive equipment are required. These equipment requirements get more stringent as the transistors get smaller.

Why is Nanotechnology important to Microelectronics? (ctd.)*

- The fabrication facilities (called “fabs”) for making these transistors get more expensive as the transistors get smaller.
- Dr. Moore also notice a trend in this cost. His observation was that the cost of building a new fab doubled every three years.
- This observation is called Moore`s Second law.

**Source : S. J. Fonash, class notes, Penn State*

Moore’s Second Law



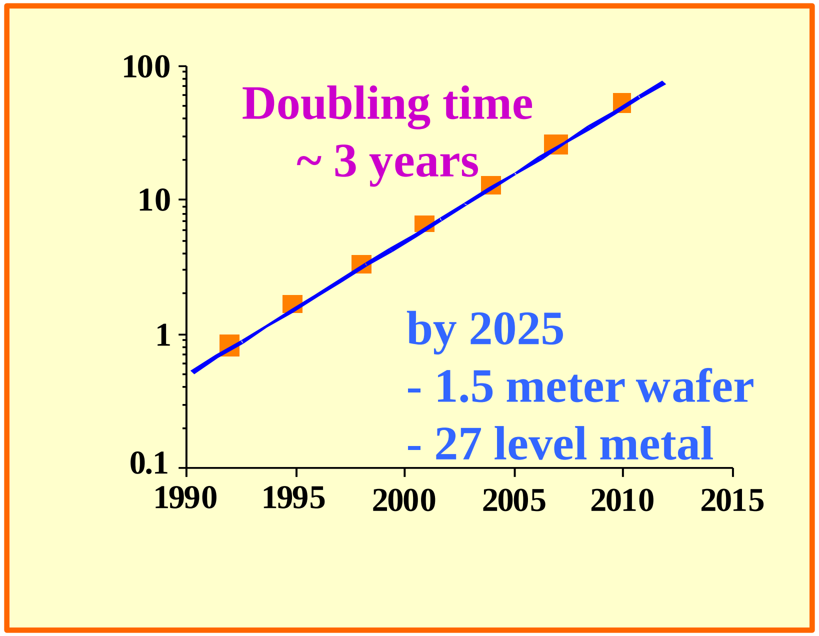
Source : Bob Trew, NCSU

*Microelectronics is not a **silicon technology** so much as it is a **lithography technology***

- <u>Problem:</u>
  - Device down-scaling and the prohibitive cost of lithography

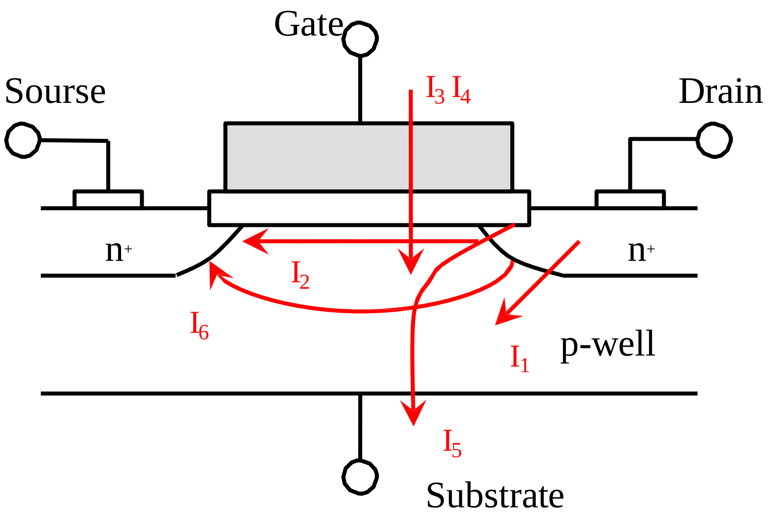
- <u>Fundamental issues:</u>
  - Devices today lithographically determined (top-down fabrication)
  - Interconnects (can not take up all the real estate)

Moore's Second Law



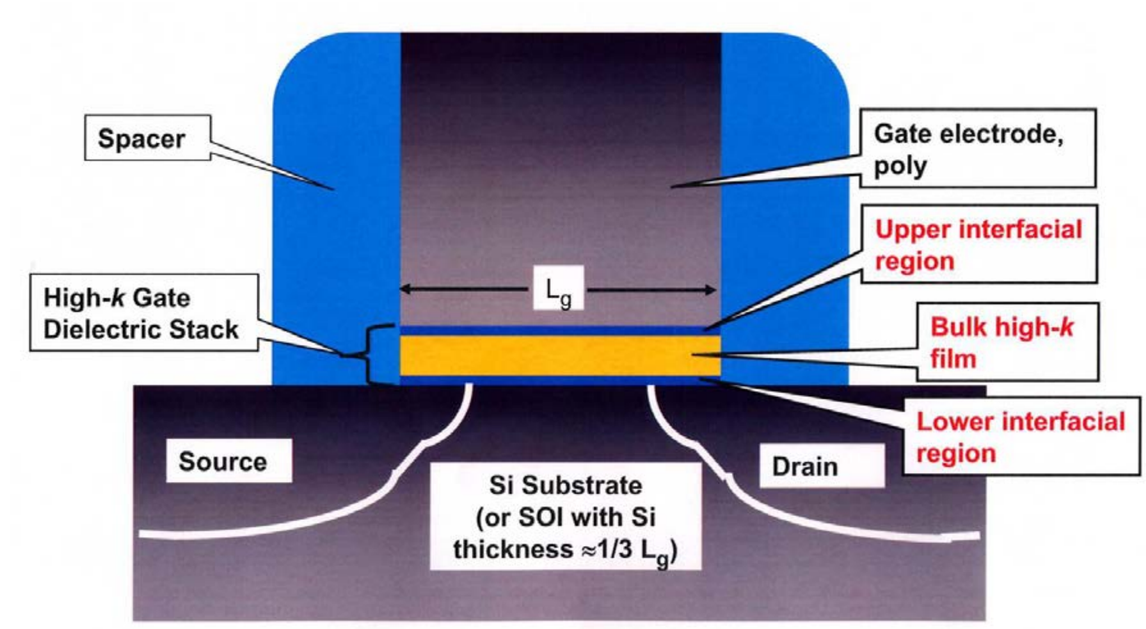
Source : Bob Trew, NCSU

Front-End of the Line Issues



- Direct tunneling and gate leakage : Thermal SiO_2 is no longer a suitable gate dielectric
  - **Problem** : as t_{ox} decreases below 30 Å quantum mechanical tunneling across SiO_2 is significantly enhanced.
  - **Solution** : use of high dielectric constant (high-k) materials for the gate dielectric instead of SiO_2.
- Potential high-k are SiN_xO_y, TiO_2, $SrTa_2O_6$, $ZrSiO_4$, HfO_2, BST etc. (k_{HK} values between 4 and 100).

High-k Materials for SiO_2 in Gate Dielectrics



$$C_{ox} = \frac{k_{ox}\varepsilon_o}{t_{ox}} A_{Gate}$$

$$k_{ox} = 3.9 \quad and \quad \varepsilon_o = 8.85\times10^{-14}\ F/cm$$

$$C_{ox} \Rightarrow C_{HK} = \frac{k_{HK}\varepsilon_o}{t_{HK}} A_{Gate}$$

$$and$$

$$Effective\ \ Oxide\ Thickness\ (EOT) = \frac{3.9}{k_{HK}} t_{HK}$$

Back-End of the Line Issues

- Conventional (IC generations of L > 0.25 μm) passivation and multilevel metallization use Al for the metal interconnects and SiO_2 (TEOS) for the interlayer dielectric (ILD).

- Problems :
  - RC interconnect delay

$$RC\ delay \propto \tau_m k_{ILD}$$

  - Power consumption

$$Power = \frac{CV^2}{2} f \propto k_{ILD}$$

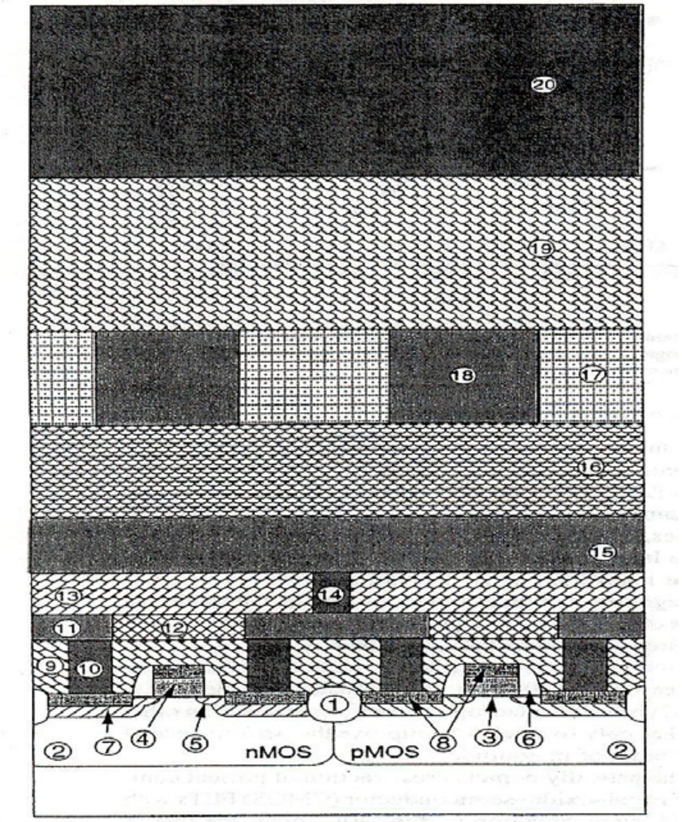
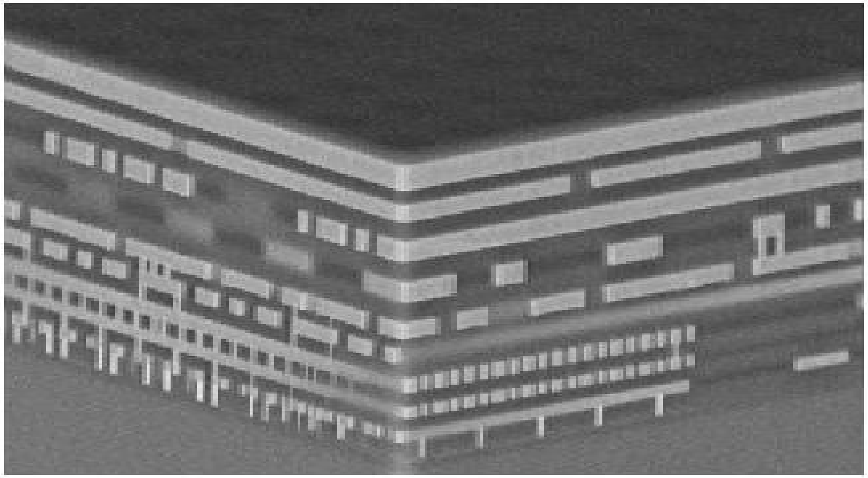


Fig. 2 Schematic cross section of present CMOS FETs with multilayered wiring.

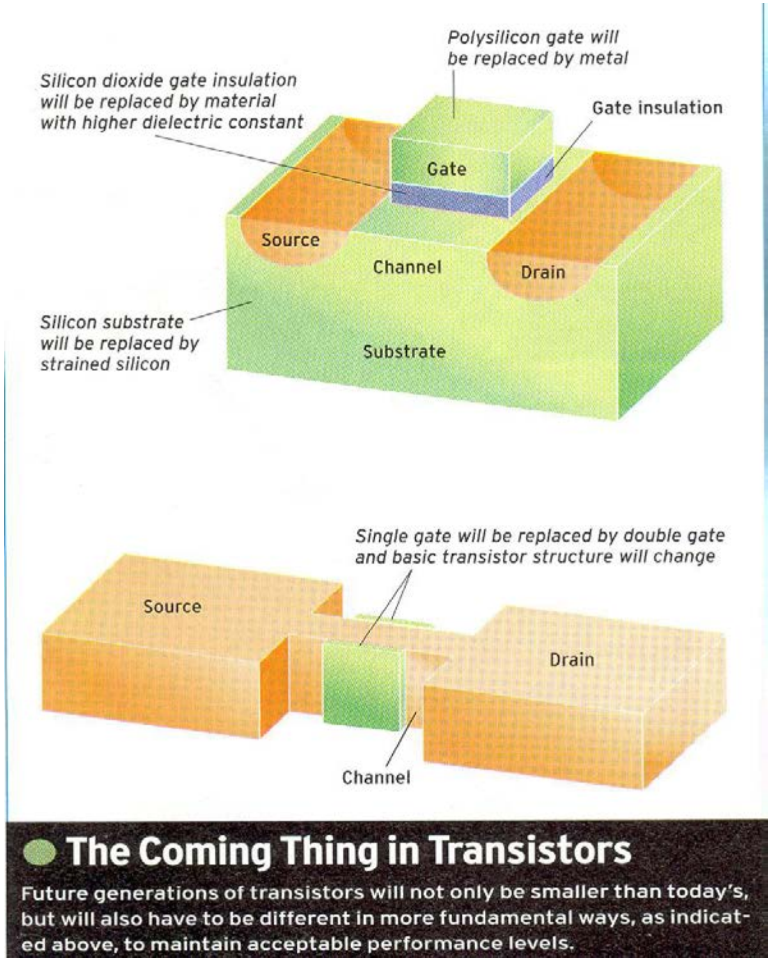
Yasuo Wada, Prospects for Single Molecule Information Processing Devices, IEEE, Vol. 89 No. 8, August 2001 Pg. 1147-1171

Solutions

- *Al is replaced by Cu .$\rho_{Al} \sim 3 - 5$ Ω cm and $\rho_{Cu} \sim 1\text{-}2$ Ω cm*
- *SiO_2 is replaced by a low-k ILD : present IC generations use low-k polymers.*



Alternatives : New Architectural Approaches



The Coming Thing in Transistors

Future generations of transistors will not only be smaller than today's, but will also have to be different in more fundamental ways, as indicated above, to maintain acceptable performance levels.

Linda Geppert, The Amazing Vanishing Transistor Act, IEEE Spectrum, October 2002, Vol. 39, Number 10, pg. 28-33

Alternatives : New Fabrication Approaches

- Many people have suggested that the microelectronics industry has to stop using top-down nanofabrication and must move to bottom-up or hybrid nanofabrication.

- If this worked, it would stop the spiraling costs of producing nano-scale transistors.

New Fabrication Approaches

- Two approaches have been proposed:
  1. Microelectronics based on nanoparticles. This has been termed <u>nanoelectronics</u>.
  2. Microelectronics based on the ultimate nanoparticles-- molecules. This has been termed <u>molecular electronics (moletronics)</u>.

Nanoelectronics

- Devices start small
  - – Nanoparticles are “born” small
  - – No need for etching
  - – Position with self-assembly; then no need for lithography
- Possible new device physics
  - – Very small structures possible—this gives rise to quantum confinement effects
  - – New types of devices possible

** Source : S. J. Fonash class notes, Penn State*

Moletronics

- Devices start very small
  - Molecules are inherently small
  - No need for etching
  - Position with self-assembly; then no need for lithography
- Possible new device physics and chemistry
  - New types of devices possible

Where are we with these alternatives?

- Generic solution proposed:
  - – Use bottom-up nanofabrication (lots of self-assembly) and avoid lithography

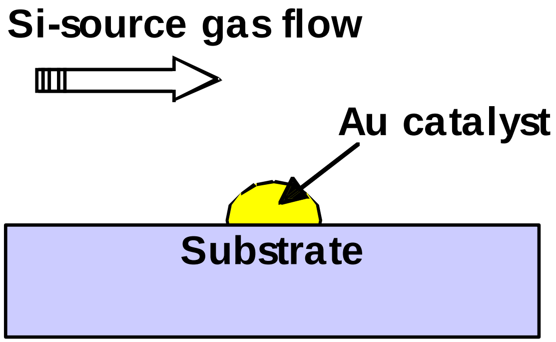
- Present state-of-the-art:
  - – Nanowire and nanotube demonstrations
  - – Molecular device demonstrations

- Challenge:
  - – Make complex self-assembled circuits

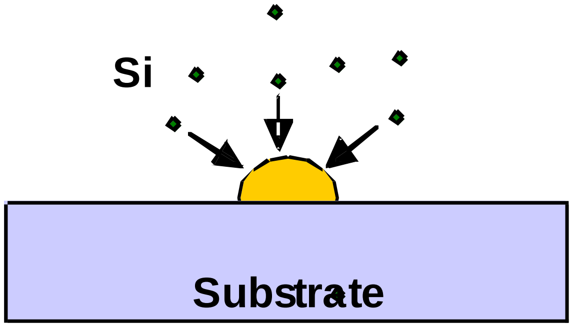
Building Blocks for Nanoelectronics

- Nanowires
- Nanotubes
- Quantum dots

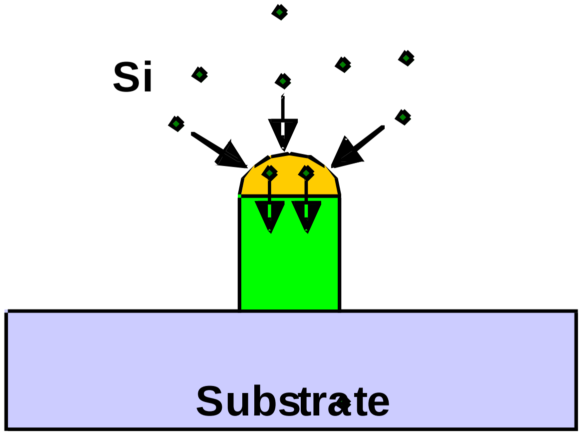
Vapor-Liquid-Solid Growth of Si Nanowires



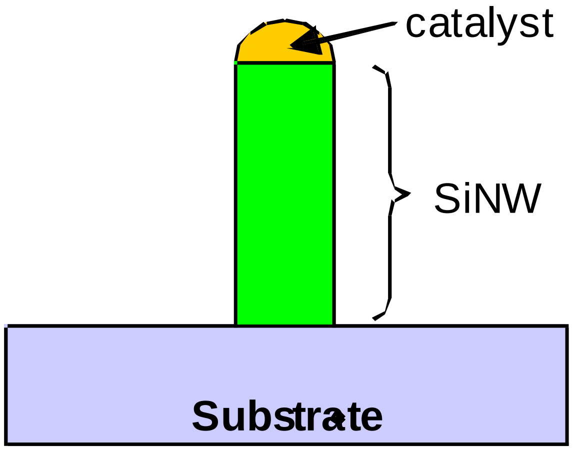
Molten eutectic alloy droplet at relatively low temperatures (363^{o}C)



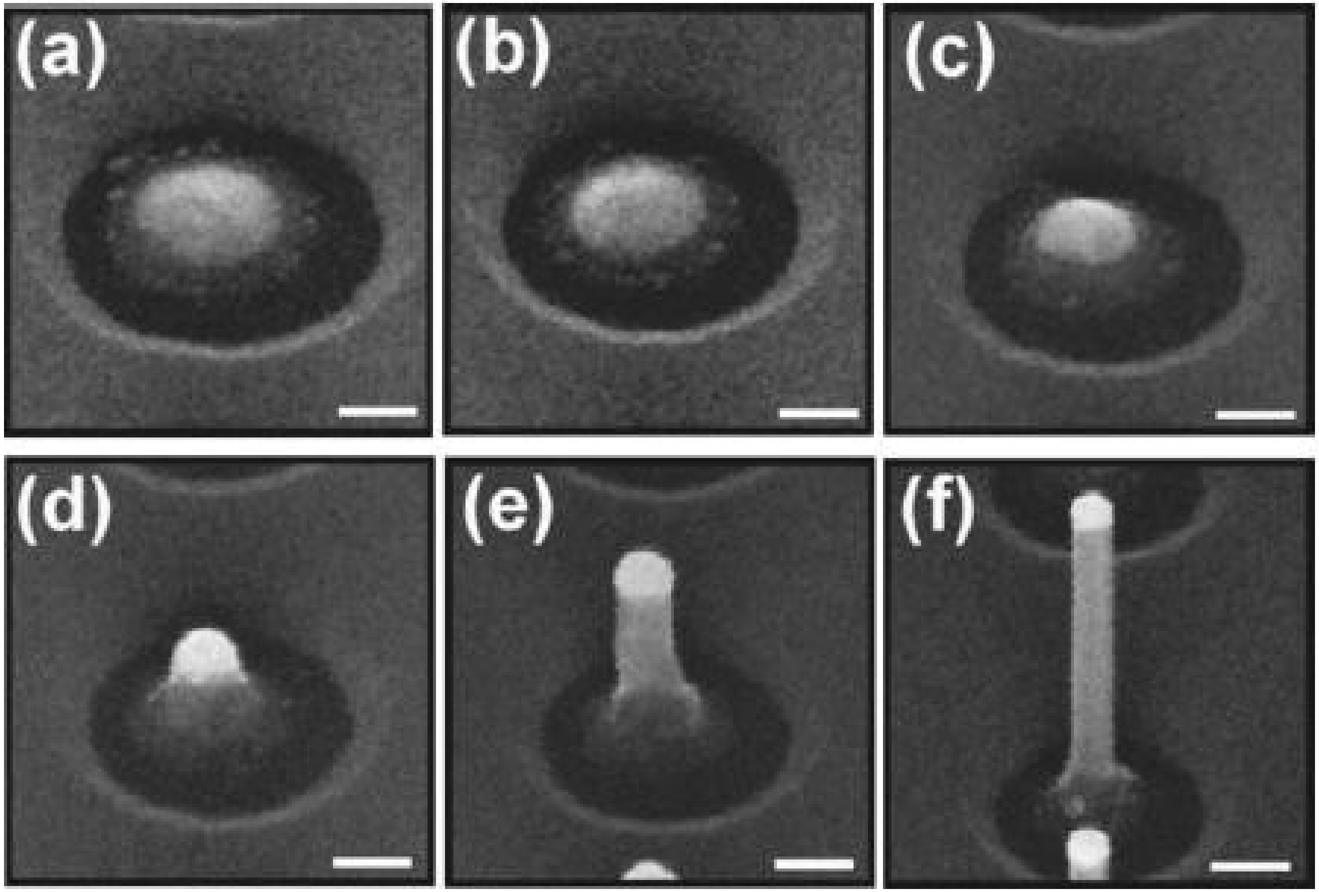
Liquid alloy acts as a preferred sink or catalyst for arriving vapor



Eutectic liquid become supersaturated and Si precipitates out at a solid-liquid interface



Nanowire grown by VLS



(J. Appl. Phys. 103, 2008, p. 024304)

Carbon Nanotubes

- Carbon nanotubes (CNTs) belong to the fullerene family. Fullerenes are composed of covalently boded C atoms arranged to form a closed, convex cage. The first of these molecules C60 was reported in Nature 1985 by Rice University team (Nobel Prize 1996). C60 distinctive soccer ball structure resembled architect Buckminster Fuller’s geodesic domes winning the name “buckminsterfullerene”.

- CNT is accredited to Sumio Iijima from NEC Corp. in 1991.

Carbon Nanotubes: Geometry

- SWNT can be imagined to be a sheet that has been wrapped into a seamless cylinder.

- A typical SWNT diameter is 1.5 nm. It is less common that SWNT diameter is 1 nm or less, and larger tubes are generally more stable than small ones.

- SWNTs might be hundreds of nm long (aspect ratios is on the order of 1000) and are closed at both ends by hemispherical caps. Half of a C60 molecule is the correct cap for large tubes.

- MWNTs are typically tens of nanometers in diameter and the spacing between the layered shells in the radial direction of the cylindrical CNT is approximately ~ 0.3 nm.

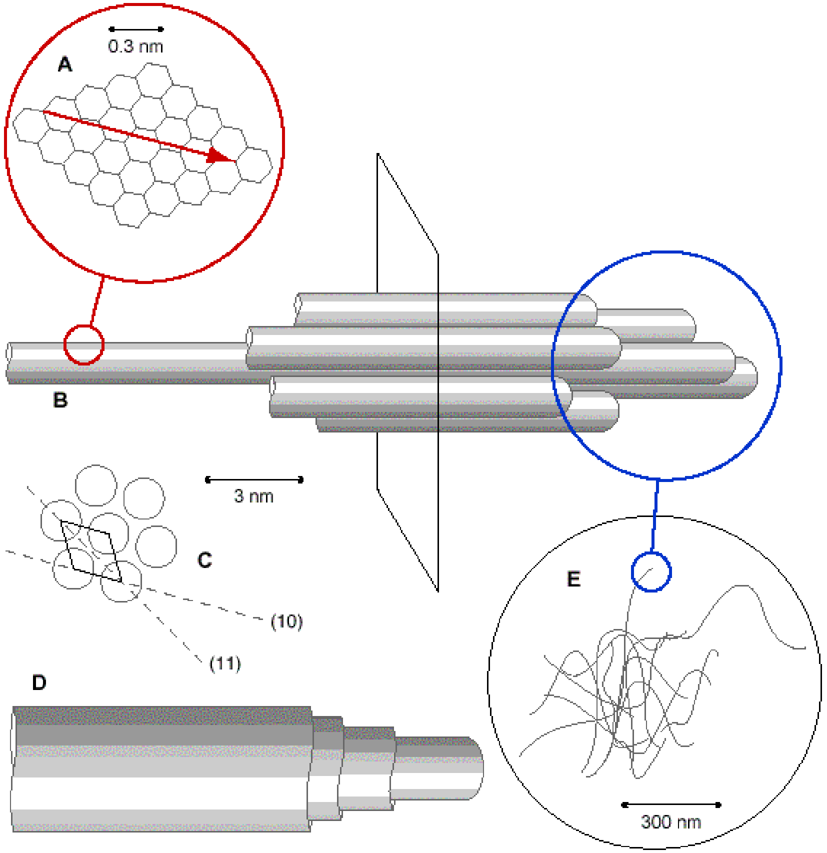
(A)The wrapping of a graphene sheet into a seamless SWNT cylinder.

(B)and **(C)** show the aggregation of SWNT in a supramolecular bundles.

The cross-sectional view in **(C)** shows that the bundles have triangular symmetry.

(D) A MWNT composed of nested SWNTs.

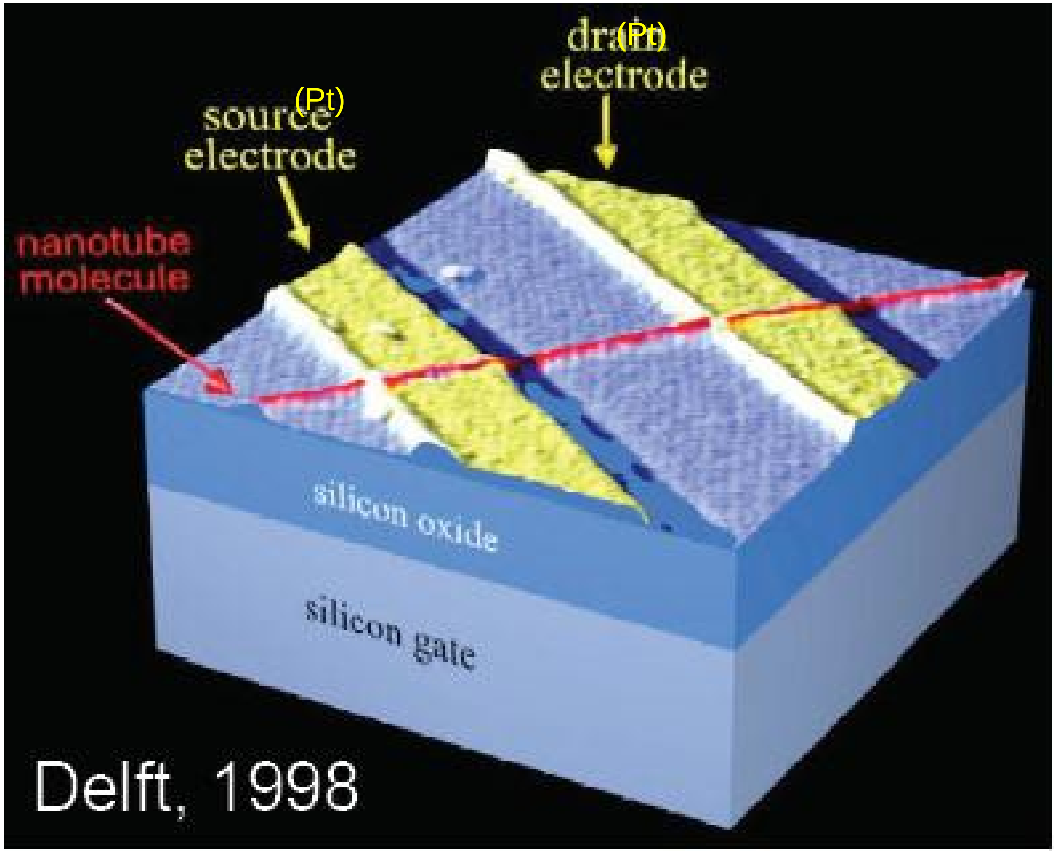
(E) At the macromolecular scale, bundles of SWNTs are entangles.



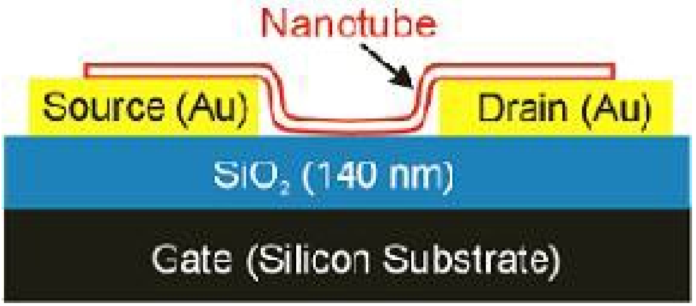
Selected Characteristics of SWNTs

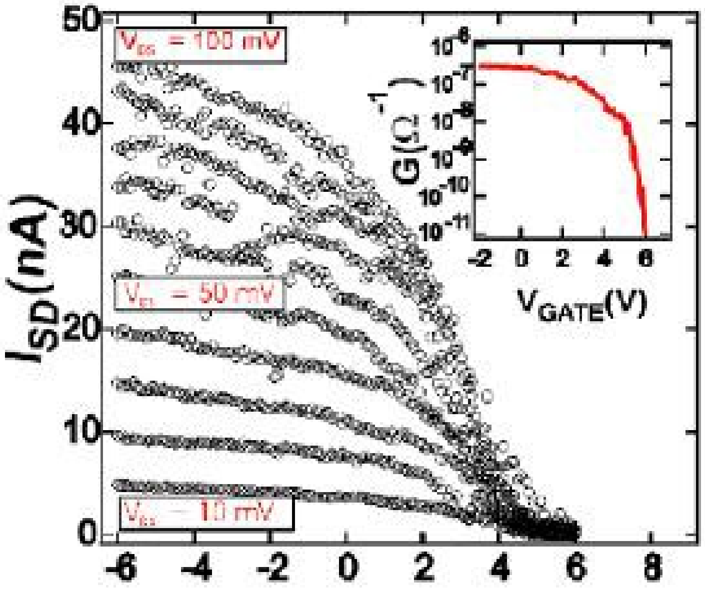
Typical diameter	*1-2 nm*
Typical length	*100-1000 nm*
Intrinsic bandgap (metallic/semiconducting)	*0 eV/~5 eV*
Work function	*~ 5 eV*
Resistivity at 300 K (metallic/semiconducting)	*10^{-4}-10^{-3} Wcm/10 Wcm*
Typical field emission current density	*10-1000 mA cm^{-2}*
Thermal conductivity at 300 K	*20-3000 W m^{-1} K^{-1}*
Elastic modulus	*1000-3000 GPa*

Carbon Nanotube Transistor



Tans, et al., Nature, 393, 49, 1998

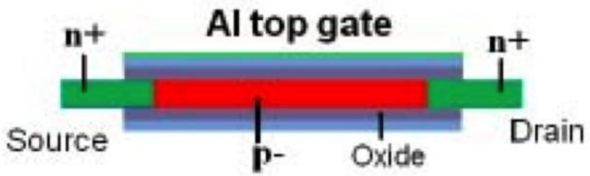


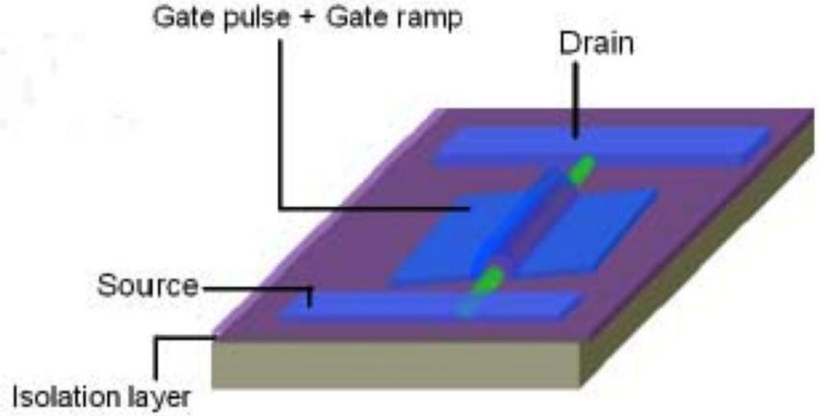


Martel et al., APL, 73, 2447,1998

Measurement of Interface States in Silicon NW Transistors

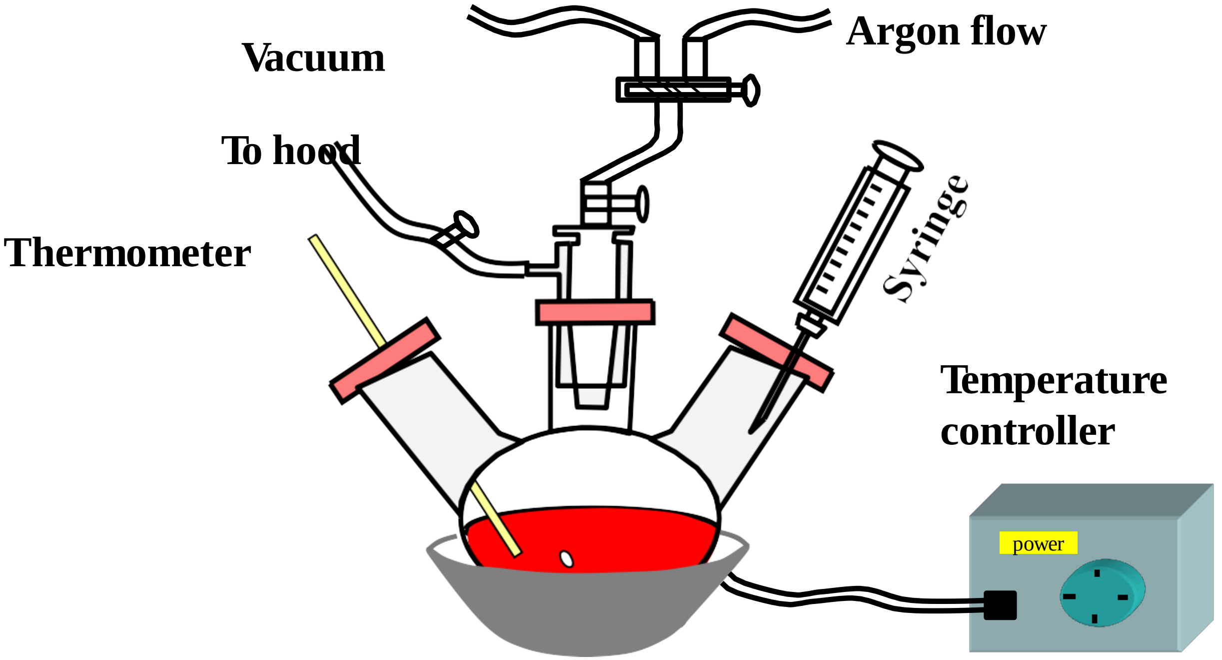
- Charge pumping (CP) is a very powerful technique for measuring interface states, D_{it}, in transistors. This is the first time a modified 3-terminal CP version (3T-CP) is applied to SiNWFETs.
- Axially doped (n^+-p^--n^+) SiNWs are grown using vapor-liquid-solid methods to a diameter ~ 46 nm as determined by FESEM.
- Oxide ground thermally in O_2 ambient at 800 C for 45 mins to form a uniform 8-nm thick shell.
- The n^+ ends of the NW are aligned onto Ti/Al contacts and a surround Al gate (200 nm) is deposited.

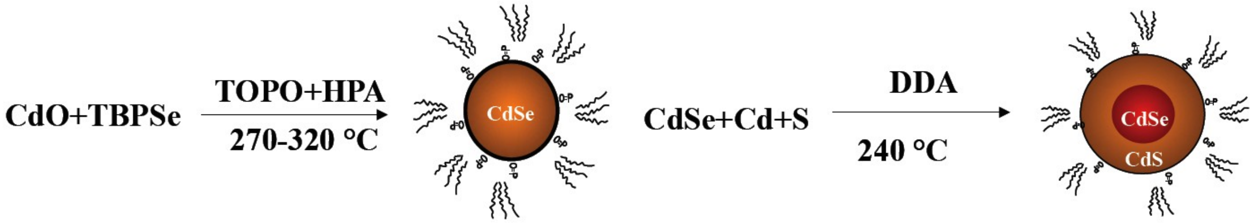




K. Sarpatwari, O. O. Awadelkarim etal., IEEE Trans. Nanotechnology, 10(4), 871 (2011)

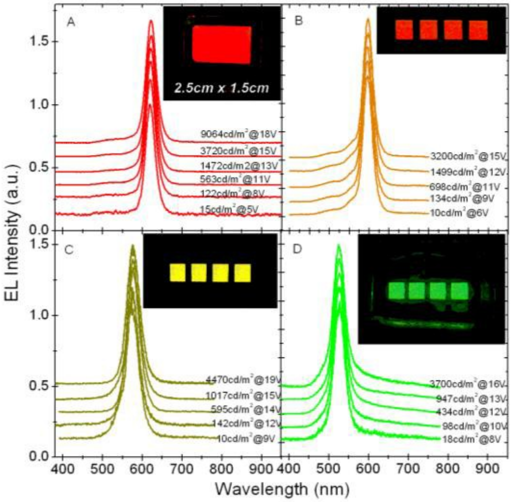
Colloidal Synthesis of Quantum Dots

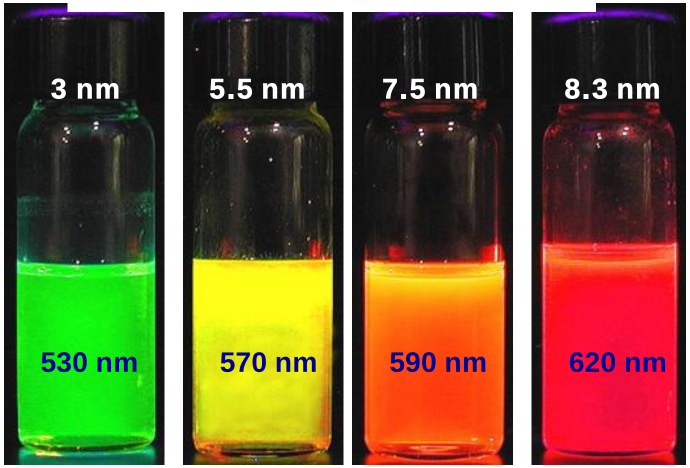




J. Xu, PSU Seminar, 2003

Semiconductor Quantum Dots: Device Quality

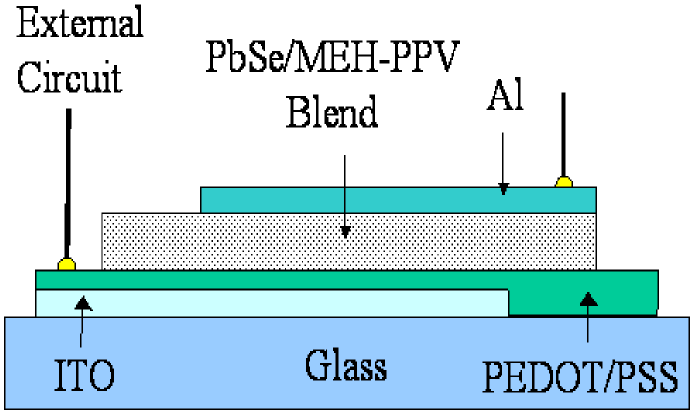


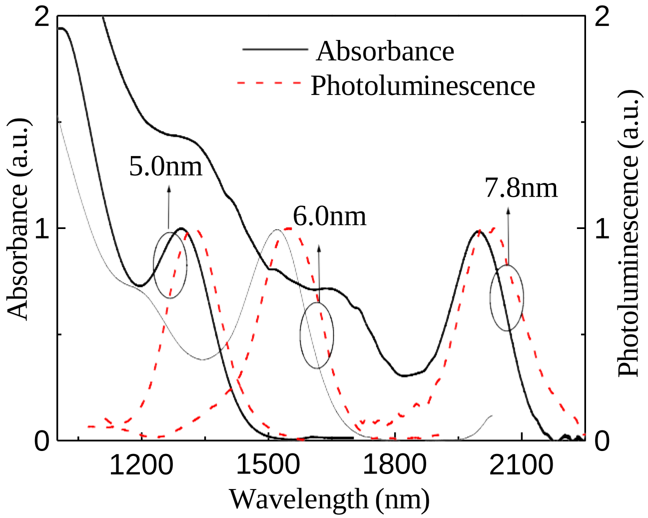


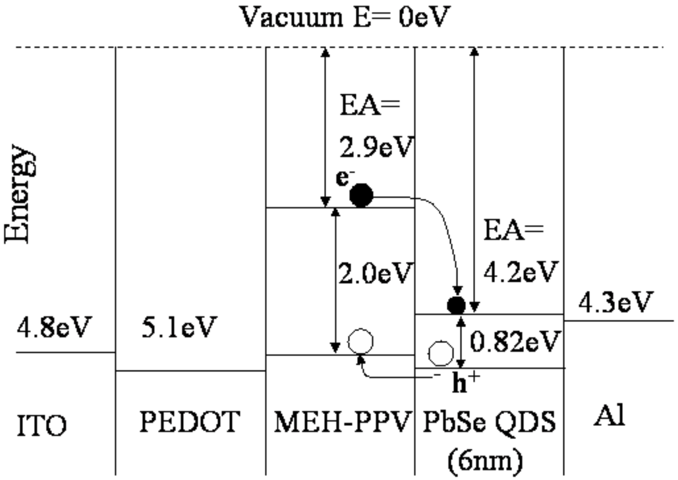
	Green QDs	**Yellow QDs**	**Orange QDs**	**Red QDs**
Core/Shell structure	CdSe/ZnS	CdSe/ZnS	CdSe/CdS/ZnS	CdSe/CdS/ZnS
Absorption (nm)	506	546	577	600
PL (nm)	527	567	589	620
FWHM (nm)	25	28	22	21
QY: as-prepared*	>70%	>70%	>70%	>70%
QY purified for QD-LED*	10 %	30%	40 %	35%

J. Xu, PSU Seminar, 2008

Solar Cells : Hybrid Infrared NQD-Polymer Photovoltaic Devices







J. Xu, PSU Seminar, 2008

Building Blocks for Moletronics

- *Molecules that show--*
  - *Reconfiguration*
  - *Redox reactions*
  - *Electron transport*
  - *Tunneling*
  - *Mechanical stress effects*

Moletronics Device Fabrication

- Hopefully self-assembly
- Probably hybrid

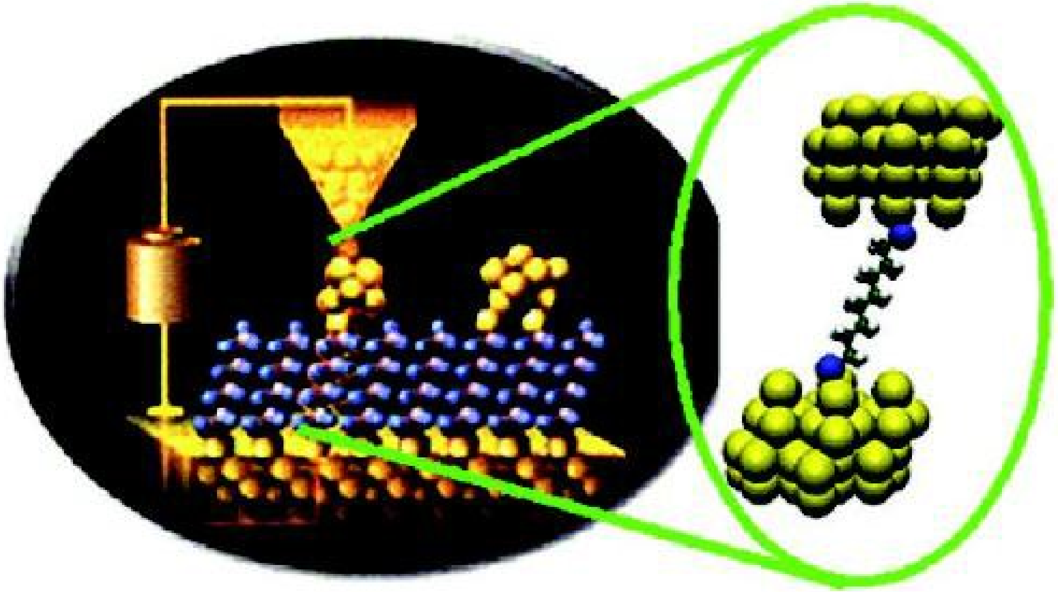


FIG. 1. The self-assembled metal-single molecule-metal junction. The molecule to be measured has a reactive thiol group at both ends and is inserted into a self-assembled alkanethiol monolayer of the same height. A gold NP is attached to the protruding thiol group at the top of the inserted molecule. A gold-coated CAFM probe is then pressed into the NP to complete the circuit. The molecule, attached to electrodes, is shown expanded on the right.

S. M. Lindsay, "Single Molecule Electronics", The Electrochemical Society Interface, Spring 2004

THANK YOU